Active Gate Control with Synthesized Signals to Avoid Overshoots and Ringing in DC-to-DC Converters

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Abstract

The high-frequency switching of power transistors causes electromagnetic disturbances and power losses in power electronic systems. In this paper, a method is presented to reduce the generation of these disturbances while maintaining a high efficiency by applying optimized gate control signals. This is realized by injecting synthesized signals to the gate via an arbitrary waveform generator and an amplifier circuit. The improved control signal is found by a heuristic optimization algorithm. The method is applied to a boost converter setup. Measurement results are presented showing the promising capabilities of the method.

1 Introduction

Power electronic systems tend to be considerable sources of electromagnetic emissions due to the high-frequency switching (ranging from kHz to MHz) of their power transistors. Ensuring a disturbance-free coexistence of other systems with power electronic systems in the electromagnetic environment is no trivial task. Without the required **e**lectro**m**agnetic **c**ompatibility (EMC) of the overall system, power electronic systems cannot be deployed.

To increase the efficiency of power electronic systems, new power transistor technologies (i.e., SiC and GaN) have been developed that enable steeper switching slopes for lower switching losses, and smaller on-resistances for lower conduction losses [1]. However, steeper switching slopes increase the electromagnetic emissions for high frequencies that may reach far into the ranges of susceptible broadcast and communication services. High-frequency ringing due to the fast switching may pose another problem. So, there is a severe conflict of interest between efficiency and EMC.

Conventional gate drivers often simply try to switch directly between two voltage levels to turn the transistor on and off, there is no feedback from the switching power transistor. A simple method for adjusting the slope of the switching waveforms are fixed gate resistors placed between driver and gate. By doing so, the switching slope is decreased and, thereby, also the generation of electromagnetic disturbances. However, this method significantly degrades the efficiency due to increased switching losses [2]. Since this approach contradicts the development of new fast-switching power transistor technologies (i.e. SiC and GaN), more sophisticated gate control techniques are required.

Active gate control techniques use more sophisticated gate drivers with, e.g., variable gate-resistances ([3] and [4]), variable input-capacitances [5], variable current sources ([6] and [7]) or variable voltage sources ([8] and [9]). There are numerous past and current publications on this topic that are comprehensively systematized and summarized in [5]. These approaches allow for a much better control of the power transistor during the switching event [5]. The required control signal can be found by different optimization methods like, e.g., simulated annealing [9], particle swarm optimization [8] and neuronal networks [11]. As a result, steep switching slopes with less oscillations and overshoots can be realized. Hereby, a better compromise between EMC and efficiency can be realized. The goal of most of the methods of active gate control is to track a target signal. Operational parameters can be, e.g., the drain-source voltage v_{ds}, the gate-source voltage v_{gs}, the drain current i_{d} or the junction temperature T_{j}. Therefore, a suitable gate control signal must be found.

In this work, a gate driving circuit using a variable voltage source is realized. There are already different implementations in this category of gate

driving circuits. One is discussed in [8] and [9] that uses cascaded inverters to adjust the gate voltage in a closed loop control. There, five inverters are connected in parallel. Therefore, a vertical resolution of $2^5 = 32$ amplitude levels of the gate control signal can be realized. The switching edge is divided in four time segments in [9]. In [8] the control signal is divided in 60 time segments. As another approach, in [10], eight resistances are connected in a star topology and can be controlled separately. Hereby, the gate voltage can be adjusted in a closed loop control with a vertical resolution of $2^8 = 256$ amplitudes for a calculated time.

In this work, in contrast to the previously described approaches of active gate control, a high-performance **a**rbitrary **w**aveform **g**enerator (AWG) and an amplifier circuit are used to generate arbitrary control signals with a high degree of freedom.

As mentioned before, the electromagnetic disturbances are generated by the switching power transistors. Finding the control signals for active gate driving is a challenging task due to the complex dynamic behavior of the power electronic system that is defined by its nonlinear and reactive characteristics. For the control of such a system, a sophisticated control strategy is needed. Here, the gate control signal is determined using a heuristic optimization algorithm.

This work is organized as follows. In Section 2, the proposed gate driving circuit and the optimization algorithm to determine the control signal are described. The demonstration setup and measurement results are discussed in Section 3. The work closes with a conclusion and outlook in Section 4.

2 Active gate control with synthesized waveforms

As stated before, the gate driving circuit shall be realized as a fast variable voltage source that is able to arbitrarily generate the needed control signals. A driving circuit is proposed and discussed. A method to define a target signal is described. The general strategy to find the required gate control signal in time domain is explained and a suitable optimization algorithm is introduced.

2.1 Proposed gate driving circuit

In this work, a high-performance AWG and an amplifier circuit are used, as depicted in Fig. 1. By doing so, the gate control signal can be synthesized more accurately and freely in comparison to the approaches in, e.g., [8] and [9]. The amplifier is used to provide the required current driving capabilities. The vertical resolution of this gate driving circuit is limited by the AWG. For the presented investigations a high-performance AWG from Tektronix, AFG3102, with 14 bit resolution and a sampling rate of 1 GS/s is used. The bandwidth of the AWG is 100 MHz. Due to the high source resistance of 50 Ohm, an amplifier ADA4870 of Analog Devices with a source resistance of 5 Ohm is added. This amplifier has a bandwidth of 52 MHz.

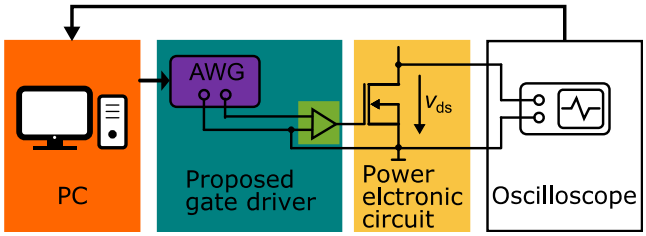

Fig. 1: Schematic of the proposed gate driver using an AWG and an amplifier

2.2 Definition of the target signal

The gate control strategy of this work is visualized in Fig. 2. The task of this approach is to generate a specific switching behavior. There are fundamentally four required steps.

In the first step, a trapezoidal PWM signal (like of a conventional gate driver) is applied to the gate of the transistor (Fig. 2 at the top left). The second step is to measure the resulting drain-source voltage v_{ds} (Fig. 2 at the top right). The aim of this work is to eliminate the overshoots of v_{ds}. Therefore, in the third step, the overshoots in the measured waveform are cut off. The resulting target waveform $v_{\mathrm{ds,t}}$ is shown at the bottom right of Fig. 2. The fourth step is to calculate the required gate-control-signal v_{cntrl} to generate the target drain-source voltage. As stated before, this shall be done by using a heuristic optimization algorithm that is described in the following.

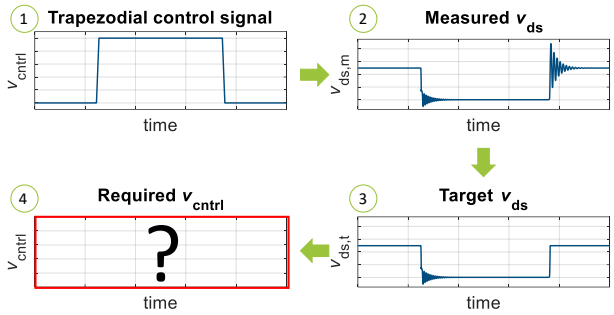

Fig. 2: Visualization of the definition of the target signal

2.3 Time-domain approach to find the required control signal

In time domain, it may be an idea to construct the gate control signal successively by considering each time step individually. However, due to the reactive behavior of the power electronic system, this approach is problematic. Time constants make it difficult to clearly evaluate the effect of the currently considered time step, and it may be required to act significantly before specific events. Therefore, it is necessary to consider the complete time period of the gate control signal during optimization. In general, there should be one optimum waveform. However, due to the numerous time and quantization steps, the number of possible permutations can be extremely high. Finding the optimum gate control waveform is a very difficult task. Potential solutions that have already been applied in other publications are, e.g., simulated annealing [9] or particle swarm optimization [8]. In this work, a heuristic approach is pursued.

2.4 Heuristic optimization algorithm

In this section, the proposed heuristic optimization algorithm is explained. The goal of this algorithm is to vary the gate control signal for the whole switching slope. If a better control signal is found, this signal is taken as the starting point for the next random variation. In each iteration, the range in which the control signal is randomly varied is reduced. This shall enable the convergence of the algorithm while avoiding local minima.

The flowchart in Fig. 4 shows the general procedure. At the beginning, all variables are initialized. In the first four steps, the target drain-source voltage is determined as described in the previous section. To adjust the switching behavior of the power transistor, only a small range around the switching edge is considered and modified.

As a starting point for the actual optimization algorithm, the trapezoidal signal of the first step is used. During the variation phase, a modification signal $v_{\mathrm{cntrl,var}}$ is added to the previously best control signal $v_{\mathrm{cntrl,best}}$, as described in Eq. (1):

$$v_{\mathrm{cntrl,test,i}} = v_{\mathrm{cntrl,best,i}} + v_{\mathrm{cntrl,var,i}}. \qquad (1)$$

The variation in the n-th iteration step is done in the range $[-A_{\mathrm{var,n}}, A_{\mathrm{var,n}}]$ separately for each optimized time step i. The limit $A_{\mathrm{var,n}}$ is decreased in each iteration step. Therefore, the variation range is successively reduced. The signal $v_{\mathrm{cntrl,var}}$ is calculated by Eq. (2) for each time step separately where $A_{\mathrm{var,n}}$ is the norm of the variation interval and $x_{\mathrm{rand,i}}$ is a random number in the range $[0,1]$:

$$v_{\mathrm{cntrl,var,i}} = -A_{\mathrm{var,n,i}} + 2 \cdot A_{\mathrm{var,n,i}} \cdot x_{\mathrm{rand,i}}\,. \qquad (2)$$

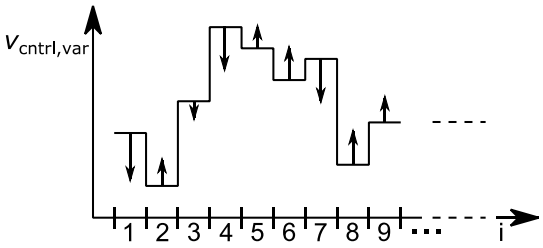

Fig. 3: Schematic illustration of the variation of each time step of $v_{\mathrm{cntrl,var}}$

A schematic illustration of the variation in each time step i is shown in Fig. 3. The resulting test signal $v_{\mathrm{cntrl,test}}$ is limited to the maximal allowed limits of the gate-source voltage in consideration of the amplification factor of the amplifier. Additionally, the determined gate control signal is low-pass filtered to avoid unnecessary voltage jumps that contain frequency components far above the AWG's and amplifier's bandwidth. In the next step, the control signal to be tested is applied to the gate, and the resulting drain-source voltage is measured. After that, the mean squared error (after the iteration n) between the target signal and measured signal $v_{\mathrm{ds,measure}}$ is calculated by equation (3):

$$error_{\mathrm{n}} = \overline{\left(v_{\mathrm{ds,measure}} - v_{\mathrm{ds,t}}\right)^2}. \qquad (3)$$

If $error_{\mathrm{n}}$ is smaller than the smallest $error_{\mathrm{best}}$ of previous iterations, the actual tested $v_{\mathrm{cntrl,var}}$ becomes the next $v_{\mathrm{cntrl,best}}$. Analog, $error_{\mathrm{n}}$ becomes $error_{\mathrm{best}}$. If $error_{\mathrm{n}}$ is higher than $error_{\mathrm{best}}$, the tested signal $v_{\mathrm{cntrl,var}}$ is discarded. Then, the iteration counter n is increased. The

optimization process is repeated until the maximal number of iterations is reached.

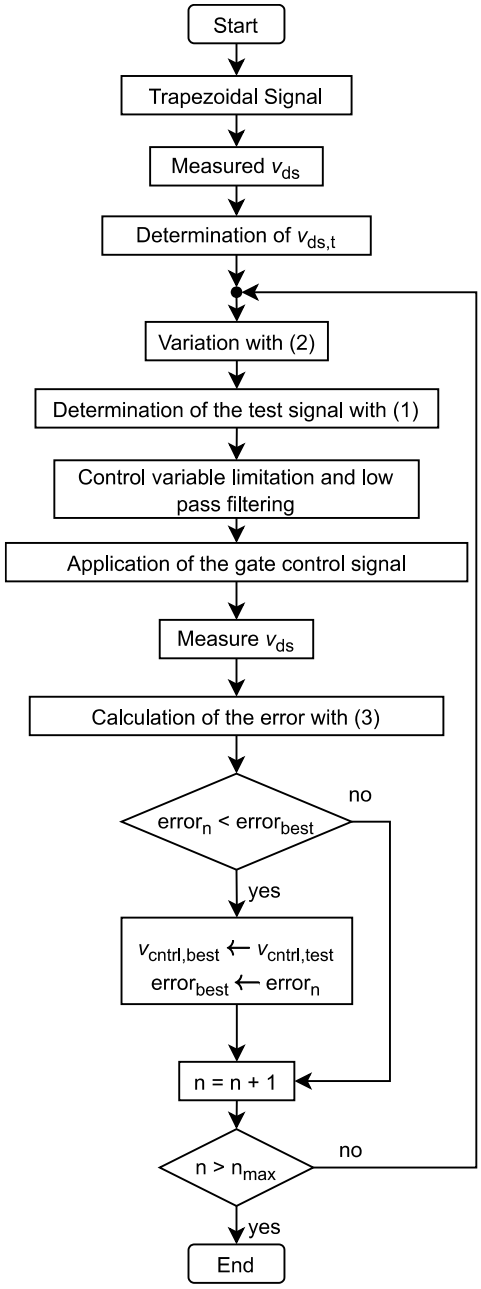

Fig. 4: Flowchart of the proposed heuristic optimization algorithm

3 Application Example

In the following, the proposed active gate driver approach is demonstrated for a DC-to-DC converter. First, the used test setup is presented. Afterward, the method to measure the power losses is described. Measurement results are discussed, and the performance of the proposed method is compared to conventional gate driver approaches.

3.1 Test Setup

The schematic of the considered boost converter is shown in Fig. 5. It boosts an input voltage V_{in} of 20 V to an output voltage V_{out} of 100 V. A switching frequency of 100 kHz and a duty cycle of 80 % are used. The MOSFET used here is an SCT3120AL of Rohm Semiconductor. For the diode, an SCS208AGC of Rohm Semiconductor is used. The input and output capacitances have values of C_{in} = 30 µF and C_{out} = 2 µF, respectively. An inductance with L = 220 µH and a load resistance of R = 94 Ω are applied. Therefore, a power of approximately 106.4 W is transferred. The DC input voltage is applied by a power supply EA-PSI 8080-340 of EA Elektro-Automatik. For measuring the drain-source voltage, a LeCroy oscilloscope Wavesurfer 3054 is used. The optimization algorithm is implemented in MATLAB and runs on a PC. As stated before, the calculated control signals are mathematically low-pass filtered with a -3 dB bandwidth of 80 MHz and a drop of 60 dB/decade before they are sent to the arbitrary waveform generator to avoid unnecessary voltage jumps. A photograph of the test setup is shown in Fig. 6.

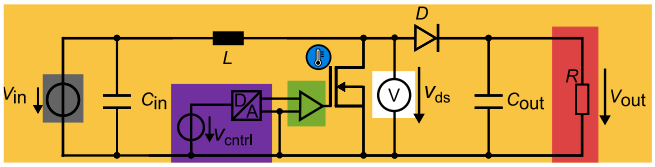

Fig. 5: Schematic of the considered boost converter

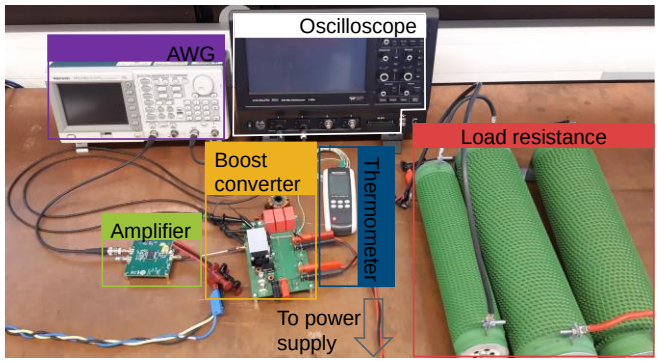

Fig. 6: Photograph of the test setup

3.2 Measurement of power losses

To evaluate the conflict of objectives between the efficiency and the EMC, the average power losses must be measured. Here, a caloric measurement of the average power losses is performed by measuring the resulting temperature. To do so, the thermal behavior of the MOSFET must be characterized. The schematic of this setup is shown in Fig. 7. A DC current is applied to the source electrode of the MOSFET while it is turned off. So, the current flows through the body diode of the MOSFET. The voltage drop over the MOSFET is measured. On the basis of the impressed current I_{test} and the measured voltage V_{test}, the average power losses P_{v} are calculated by

$$P_{\mathrm{v}} = V_{\mathrm{test}} \cdot I_{\mathrm{test}}. \tag{4}$$

Simultaneously, the temperature of the MOSFET is measured using a thermocouple. The relation between the measured temperature and the average power losses is shown in Fig. 8. This serves as the basis for the determination of the power losses in later steps. Using this relationship, the power losses of the MOSFET can be determined by measuring its temperature.

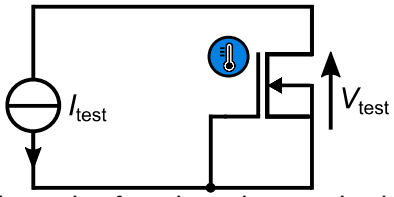

Fig. 7: Schematic for the characterization of the MOSFET's thermal behavior

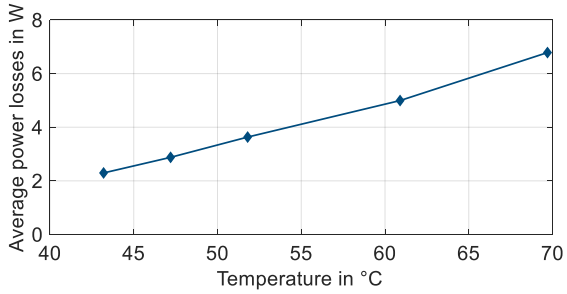

Fig. 8: Relation between the measured temperature and the corresponding average power losses

3.3 Exemplary Measurement results

In this section, the measurement results are presented. First, the original gate control signal (trapezoidal but low-pass filtered) is generated by the AWG and applied to the gate of the transistor via the amplifier. This test signal is shown in Fig. 9 in blue. The corresponding drain-source voltage is shown in Fig. 10 in blue. It can be seen that the maximal overshoot (voltage over 94V) has a value of 43.5 V.

On the basis of the measured v_{ds}, the target drain-source voltage is determined. The drain-source voltage is depicted in Fig. 10 in red and should have no overshoot anymore. Then, the optimization is performed that should optimize the control voltage accordingly. Here, the search range of the optimization algorithm starts at $A_{\mathrm{var,max}}$ of 1 V and is decreased to $A_{\mathrm{var,min}}$ of 0.01 V within 300 iterations. The resulting gate control signal and the corresponding drain-source voltage are illustrated in Fig. 9 and Fig. 10 in yellow.

A reduction of the overshoot to zero could not be achieved, but it is reduced by 60 % to 17 V. Using the original control signal, the transistor has a temperature of 55 °C. The original power losses can be determined to 4.1 W by using the relationship of Fig. 8. Applying the optimized gate control signal, a temperature of 59.8 C can be measured. This is corresponding to average power losses of 4.8 W. Therefore, applying the proposed optimization algorithm reduces the overshoots by 26.5 V, but increases the average power losses by 0.7 W.

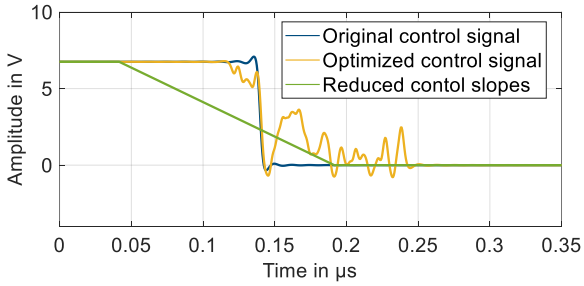

Fig. 9: Original control signal, optimized control signal, and control signal with reduced slopes

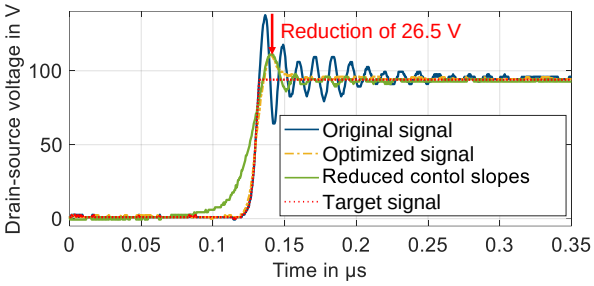

Fig. 10: Original drain-source voltage, optimized drain-source voltage, drain-source voltage with reduced control slopes and target drain-source voltage

Now, the proposed method shall be compared to conventional gate drivers. As mentioned before,

the overshoots can be reduced by using an additional gate-resistance. This can be replicated by reducing the voltage slope of the trapezoidal gate control signal. To generate the same maximal overshoot, the switching slope must be extended from 3 ns to 150 ns. The resulting gate control signal and the measured drain-source voltage are shown in Fig. 9 and Fig. 10 in green. In this case, the temperature is increased to 61 °C resulting in power losses of 5.0 W. In comparison, the proposed method causes power losses of only 4.8 W. So, by applying the proposed method, the power losses are decreased by 0.2 W while achieving the same overshoot.

3.4 Pareto frontiers

Last, the Pareto frontiers are considered. The Pareto-optimal front of a conventional gate driver (replicated by trapezoidal waveforms with different voltage slopes) is depicted in Fig. 11 in blue. Using the proposed method, the power losses can be reduced by up to 0.56 W while ensuring the same maximal overshoot. Considering the transfer power of approximately 106.4 W, the efficiency can be improved by approximately 0.52 %. For the same power losses, the maximum overshoot can be reduced by 3.1 V. Therefore, the proposed method offers the potential to improve the conflict of objectives between the reduction of overshoots and the efficiency.

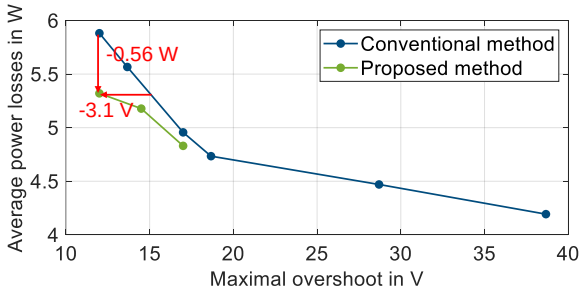

Fig. 11: Pareto-optimal frontier of a conventional gate driver in comparison to the proposed method

4 Conclusion and outlook

Power electronic systems are potential sources of electromagnetic disturbances. To avoid the generation of these disturbances, the switching slopes of power transistors can be decreased by increasing, e.g., the gate resistors of conventional gate drivers. Since this measure may increase the power losses, there is a severe conflict of objectives. In this work, an active gate control is applied that offers a reduction of overshoots without significantly reducing the switching slopes. The driving circuit is realized by an arbitrary waveform generator and an amplifier to precisely generate the control signal with a high degree of freedom. The required control signals are found by a heuristic optimization algorithm. This active gate control is applied to a DC-to-DC converter. The drain-source voltage overshoots are significantly reduced by 60 %. In comparison to conventional approaches, the achieved efficiency is 0.52 % higher. The Pareto frontier of the proposed method shows a better performance than the one of conventional approaches and may offer new, optimized solutions for power electronic systems.

In future, the simple heuristic optimization algorithm may be extended and improved to achieve better results after less iterations.

5 References:

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