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FPGA-based Active Cancellation of the EMI of a Boost Power Factor Correction (PFC) by Injecting Modulated Sine Waves

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***Abstract*—Boost power factor corrections tend to be considerable sources of electromagnetic disturbances. To ensure the proper functionality of susceptible systems in the vicinity, the emissions must be reduced. Passive filters, as a conventional solution to reduce conducted emissions, usually suffer from their high volume, weight and costs. Active filters can help to mitigate this problem, but the known solutions are systematically limited by inherent time constants and signal propagation delays since they derive the cancellation signal directly from a measured quantity by a feedforward and/or feedback approach. To resolve this issue, each harmonic can be individually suppressed by an artificially synthesized sine wave that is synchronized to the disturbances. By adjusting the amplitudes and phases of the suppressing sine waves, bothersome time constants and delay times can be compensated. In this work, it is shown that the switching harmonics of a power factor correction can be interpreted as modulated sine waves. By modulating the suppressing sine waves simultaneously, a very high performance can be achieved for the active cancellation system. The hardware and the algorithm are described, optimum parameters for the algorithm are identified and an FPGA implementation is applied to a real PFC.**

***Index Terms*—EMI, PFC, cancellation, synthesized signals, modulated signals, FPGA**

I. Introduction

Power **f**actor **c**orrections (PFCs) are typical first stages of mains-operated devices to increase the name-giving power factor. This is done by drawing a current with the same waveform (ideally a sine with, e.g., 50 or 60 Hz) and same phase as the voltage from the mains. Boost PFCs comprise a full-bridge rectifier and a boost converter. The **p**ulse-**w**idth **m**odulated (PWM) control signals of the boost converter are regulated by feedback loops to maximize the power factor and to generate a DC voltage at the output.

The switching operation of the PFC's boost converter may cause

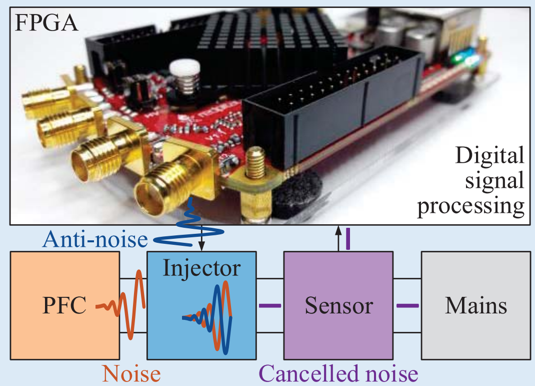

Fig. 1: Active EMI cancellation using digital signal processing.

high-frequency **e**lectro**m**agnetic **i**nterferences (EMI) with significant power levels. This EMI may propagate through the supply lines into the mains and cause disturbances in susceptible systems. To avoid this problem, the conducted EMI is usually attenuated by using passive EMI filters [1]. However, these elements tend to be large, heavy and expensive in comparison to the power electronics itself. Methods of active EMI cancellation can help to resolve this problem.

Until now, **a**ctive **E**MI **f**ilters (AEFs) have been applied that generate the cancellation signal from the measured EMI by a feedforward and/or feedback approach (e.g. [2]-[7]). However, these approaches are systematically limited since the generated anti-EMI will never be exactly simultaneous with the EMI due to, e.g., time constants and signal propagation delays [8].

To resolve the limitations of feedforward and feedback approaches, the cancellation signal for quasi-periodic EMI can be **artificially synthesized** from sine waves (e.g. [8]-[10]). By **adaptively** adjusting

Take-Home Messages:

- Boost PFCs generate a large number of sideband harmonics adjacent to the switching harmonics.
- In time domain, the switching harmonics with their adjacent sideband harmonics can be interpreted as modulated sine waves.
- For active cancellation of these disturbances, modulated sine waves can be injected into the system.
- The generation of the modulated sine waves for cancellation can be done by, e.g., an FPGA system with analog-to-digital and digital-to-analog converters.
- The usage of artificially synthesized, synchronously modulated sine waves can achieve high EMI reductions (about 40 dB) up to at least 1 MHz.

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the amplitudes and phases of each sine wave, the influence of time constants and delay times can be compensated. This adjustment can be done by appropriate **optimizers** that observe the residual EMI (superposition of EMI and anti-EMI). In this work, a specialized optimization and synthesis method is proposed that can be applied to the typical EMI of a boost PFC.

At first, the topology and characteristic emissions of a boost PFC are discussed. Afterward, a digital active EMI cancellation system is proposed (Fig. 1). The topology is described, and the algorithm is discussed. Optimum parameters for the algorithm are found by a systematic investigation. This cancellation system is applied to a PFC evaluation board. The results are presented and briefly discussed. The work is closed by a conclusion.

II. Topology and EMI of a Boost PFC

In this section, the topology of the considered PFC is presented. Furthermore, the EMI resulting from the PWM switching of the boost converter is discussed.

A. Topology

The topology of the considered PFC is depicted in Fig. 2. The full-bridge rectifier generates a pulsating DC voltage $|v_{\text{mains}}(t)|$ from the mains voltage $v_{\text{mains}}(t)$. The duty cycle of the boost converter is controlled by feedback loops (not depicted here) in such manner that the output voltage V_{output} is constant at the desired voltage level and that the current $i_{\text{mains}}(t)$ follows the mains voltage $v_{\text{mains}}(t)$ without phase shift.

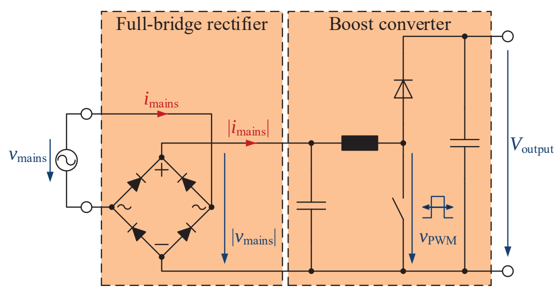

Fig. 2: Topology of the considered boost PFC.

B. EMI Resulting from the PWM

A typical PWM signal of the switching node's voltage $v_{\text{PWM}}(t)$ is depicted in Fig. 3 (top plot). For better visibility, the switching frequency is chosen to be much lower than usual in this depiction. The duty cycle is varied over time by the above-mentioned control loops. The resulting spectrum can be found in Fig. 4. The fundamental harmonic at the switching frequency f_{PWM} and its overtones at $2f_{\text{PWM}}$ and $3f_{\text{PWM}}$ can be clearly distinguished. The modulation of the duty cycle results in a large number of sideband harmonics [11]. Since the spacing between these sideband harmonics predominantly corresponds to the rectified mains frequency (e.g. 100 or 120 Hz), they are not visible with usual measurement bandwidths (e.g. 9 kHz). The switching harmonics with their adjacent sideband harmonics are brought back into time domain and depicted in Fig. 3 (lower three plots). In this representation, it is visible that the PWM signal consists of modulated sine waves. So, the resulting EMI may also be suppressed by the injection of synchronously modulated sine waves.

III. Digital Cancellation Signal Synthesis

In this section, a digital cancellation system is proposed that can

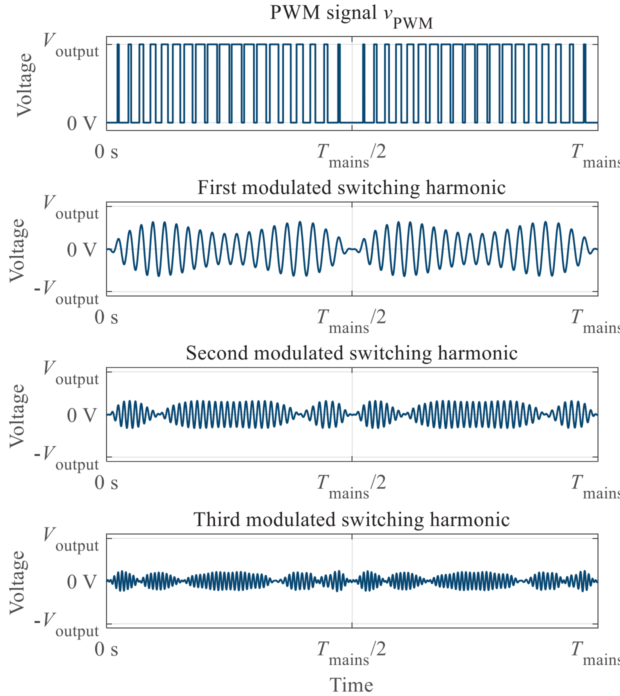

Fig. 3: Typical PWM signal of the considered PFC, modulated switching harmonics.

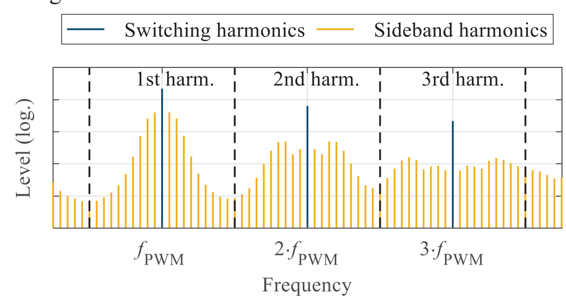

Fig. 4: Typical spectrum of the considered PFC.

generate the modulated sine waves for the cancellation of the modulated switching harmonics. At first, the topology and the hardware are presented. Afterward, the used algorithm is summarized. The parametrization of the algorithm is systematically investigated for the given application.

A. Hardware for Cancellation Signal Generation

The topology of the PFC with the active EMI cancellation system can be found in Fig. 5. The PFC is the EMI source, and the mains is the EMI victim. The high-frequency (residual) EMI at the mains is passed by an analog coupling circuit (sensor) to the cancellation system's analog-to-digital converter. The sensor rejects the operating currents and voltages of the power electronic system that could otherwise destroy the cancellation hardware. The measured signal is digitized by the analog-to-digital converter and passed to a digital optimizer. The optimizer aims at a minimization of the residual EMI by adjusting the parameters for the synthesis of the cancellation signal. The cancellation signal is generated from the found parameters by a digital synthesizer, digital-to-analog converted and passed through an analog coupling circuit (injector) into the power lines. The injector rejects the operating currents and voltages of the power electronic system as well. The injected signal should flow to the sensor and the mains. Depending on the injecting circuit and the impedances, the signal may be diverted into the PFC. To correct the impedance ratios, a decoupling circuit can be applied [8]. The PFC and synthesizer are synchronized by appropriate means: The synthesizer may be synchronized to the PFC by, e.g., the control signals of the PFC's boost converter. However, the synthesizer may also provide the clock for the PFC's boost converter to achieve the required synchronicity.

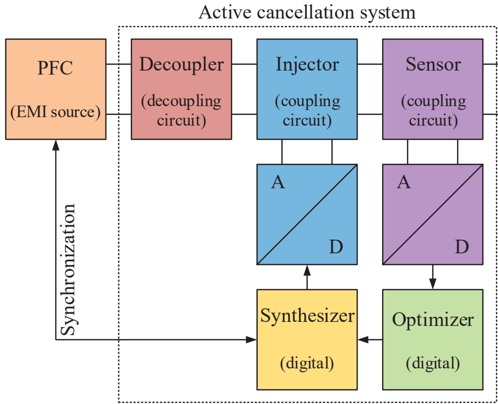

Fig. 5: Topology of the PFC and active EMI cancellation system.

B. Algorithm

The algorithm applied in this work is the so-called single-frequency adaptive notch filter with delayed LMS (**L**east-**M**ean-**S**quares) algorithm that is already well established in active noise control in acoustics [12]. This algorithm is very effective and relatively easy to implement. The fundamental structure is depicted in Fig. 6.

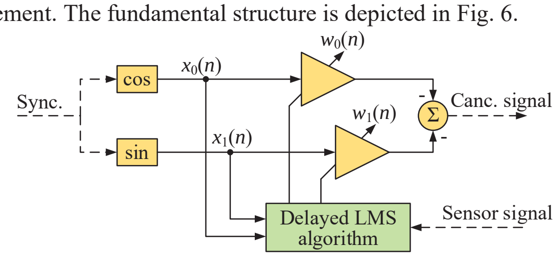

Fig. 6: Single-frequency adaptive notch filter with delayed LMS algorithm.

To be able to continuously modify the cancelling sine wave for one switching harmonic (and its adjacent sideband harmonics), an orthogonal system of a cosine and sine with the equivalent frequency is generated. These signals are synchronized (frequency- and phase-locked) to the operation of the power electronic system and defined as:

$$x_0(n) = A \cdot \cos\left(2\pi \frac{k f_{\mathrm{PWM}}}{f_{\mathrm{s}}} \cdot n\right) \qquad (1)$$

and

$$x_1(n) = A \cdot \sin\left(2\pi \frac{k f_{\mathrm{PWM}}}{f_{\mathrm{s}}} \cdot n\right) \qquad (2)$$

A is an arbitrary amplitude, k denotes the number of the considered harmonic, f_{PWM} is the switching frequency, f_{s} is the sampling rate and n is the discrete time base. The cosine and sine of the orthogonal system are respectively weighted by the factors $w_0(n)$ and $w_1(n)$, and superposed (Fig. 6). The result is a sine wave with the same frequency, but an arbitrary amplitude and phase. The negative signs at the summation element of Fig. 6 are required for consistency with the existing theory (e.g. [12]).

During operation of the PFC, the factors $w_0(n)$ and $w_1(n)$ must be continuously adapted so that the generated sine wave follows the modulated harmonics of the PWM signal. This adaption is done by the delayed LMS algorithm that minimizes the residual EMI in each sample step by using a gradient descent approach. The factors $w_0(n)$ and $w_1(n)$ are iteratively adjusted in each sample step by the following update rules:

$$w_0(n+1) = w_0(n) + \mu \cdot x_0(n-\Delta) \cdot e(n) \qquad (3)$$

and

$$w_1(n+1) = w_1(n) + \mu \cdot x_1(n-\Delta) \cdot e(n) \qquad (4)$$

In these formulas, μ is the step size of the algorithm and $e(n)$ is the residual EMI measured by the sensor. For the stability of the algorithm, the propagation delay of the cancellation signal must be respected in the update rule by the estimation Δ (in samples). This propagation delay consists of the following portions: digital-to-analog conversion, injection, propagation from injector to sensor, sensing, analog-to-digital conversion, and digital signal processing. There are many options to find the right value for Δ: The simplest way may be to find the value by trial-and-error (done here). However, it is also possible to do, e.g., an online estimation by using an additional notch filter to identify the system's behavior [12]. The actual delay time should be as short as possible so that the algorithm has a shorter dead time and, therefore, a better dynamic behavior.

To suppress multiple switching harmonics with their adjacent sideband harmonics, the structure of Fig. 6 can be implemented several times in parallel. The delayed LMS algorithm always uses the unfiltered sensor signal for optimization. The synthesized and modulated sine waves can be superposed in digital domain to form one broadband cancellation signal. Therefore, it is sufficient to use only one injector and one sensor. [9],[10]

C. Optimal Step Size for the Given FPGA System

The step size μ defines the convergence rate of the algorithm. In the given application, the algorithm must be fast enough to follow the changes of the PWM signal. However, the algorithm may become imprecise or even unstable if the step size is too large. So, the optimum must be found.

For a parameter study of the step size μ, the PWM signal of the considered PFC is emulated using an FPGA system Red Pitaya STEMlab 125-14 (Fig. 1). The switching frequency is set to 100 kHz and the mains frequency is assumed to be 50 Hz. Due to an assumed mains voltage of 230 V and an assumed DC output voltage of 400 V, the duty cycle is varied between 0% and approximately 81%. The optimization and synthesis of the cancellation signal is realized on the same FPGA system to achieve the required synchronicity between the disturbing and cancelling signal. The emulated EMI and the generated anti-EMI are both digital-to-analog converted and superposed by a 50 Ω power splitter. For the optimization of the cancellation signal, the resulting residual EMI is analog-to-digital converted and passed to the FPGA. The FPGA system uses a sampling rate of 125 MS/s. The analog-to-digital and digital-to-analog converters have a vertical resolution of 14 bit. In total, the converters introduce a delay time of approximately 112 ns. This value is set for the delay time estimation ($\Delta = 112\,\mathrm{ns} \cdot 125\ \mathrm{MS/s} = 14$). To check the performance of the active cancellation system, the residual EMI is evaluated by using an EMI test receiver with a resolution bandwidth of 9 kHz, a measurement time of 50 ms and an average detector.

The achieved EMI reduction for the switching harmonics (with adjacent sideband harmonics) at 100 kHz and 1 MHz can be found in Fig. 7. As expected, there are optimum step sizes that allow the cancellation signal to follow the changes of the PWM signal without becoming too imprecise. Too small step sizes result in a too slow convergence that cannot keep up with the changes of the PWM signal. Too large step sizes make the algorithm imprecise or even unstable. It can be found that the optimum step size for 100 kHz ($\mu = 6.7 \cdot 10^{-3}$)

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is much smaller than the one for 1 MHz ($\mu = 5.0 \cdot 10^{-2}$). This is due to the fact that the modulation of the duty cycle has a smaller impact on the first switching harmonics and a much larger on the higher ones. Therefore, the algorithm must be much faster for higher frequencies. All in all, active EMI reductions of 40 dB are within reach for frequencies of at least 1 MHz.

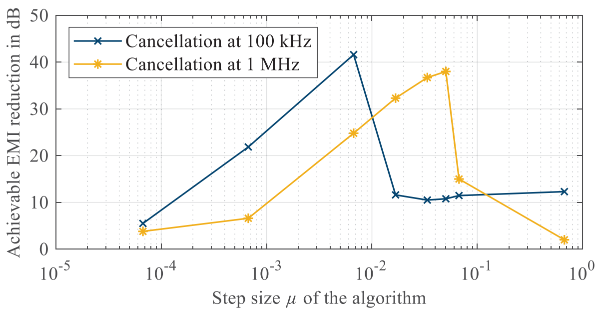

Fig. 7: Investigation of the achievable EMI reduction in respect to the step size μ of the algorithm.

IV. Demonstration

Last, the algorithm (with optimum step size) is applied to the fundamental wave (100 kHz) of a PFC evaluation system IPP60R190P6 from Infineon in the configuration of Fig. 5. The mains voltage is 230 V with a frequency of 50 Hz. The PFC is operated with a transfer power of roughly 223 W. The active cancellation system is still implemented on an FPGA system Red Pitaya STEMlab 125-14. For synchronization, the PFC uses a 100 kHz reference signal from the FPGA system as basis for its switching frequency.

The cancellation system is used to suppress the differential-mode EMI at the input of the PFC. The injector and sensor use a capacitive coupling with 100 nF capacitors. A low-pass filter with a cut-off frequency of 2.5 MHz is installed between the sensor and the analog-to-digital converter to avoid an overdrive due to the high-frequency ringing caused by the PFC's switches. Attenuators (50 Ω) are applied to the analog-to-digital and digital-to-analog converters to adjust voltage ranges and to match impedances. The cancellation system injects a current that is split between the PFC and the mains. Since the PFC has a much lower input impedance than the mains, most of the injected current would not support the active cancellation at the mains. To resolve this issue, the high-frequency impedance of the PFC is increased by applying a split core ferrite MnZn 74272733 from Würth Elektronik with 1.5 windings of the supply line as a decoupler. The EMI test receiver measures the DM EMI at a **l**ine **i**mpedance **s**tabilization **n**etwork (LISN) with a measurement time of 50 ms, a resolution bandwidth of 9 kHz and an average detector.

The measurement results for this prototype test system are depicted in Fig. 8. The frequency range is limited to 1 MHz for a clear depiction of the effect on the first switching harmonics (with their respective sideband harmonics). The installation of the injector, sensor and decoupler passively attenuates the disturbances by approximately 3 dB at 100 kHz. After activating the cancellation system, the disturbances at 100 kHz are actively suppressed by additional 39 dB. As intended, there is only a marginal effect on the other switching harmonics. Similar results have been found for the peak emissions.

V. Conclusion

In this work, a specialized optimization and synthesis method has been proposed to actively cancel out the disturbances of a boost PFC

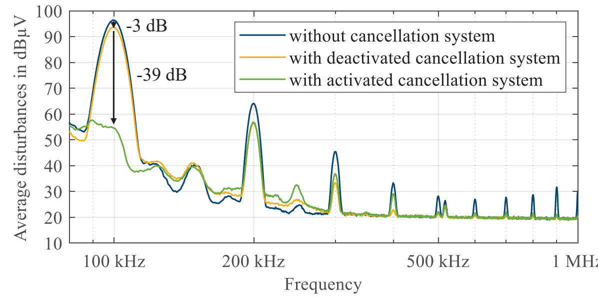

Fig. 8: Measurement results for a PFC evaluation system.

by injecting artificially synthesized and modulated sine waves. It has been shown that the switching harmonics are spread out in frequency domain by the time-varying PWM control scheme. The switching harmonics with their adjacent sideband harmonics can be interpreted as modulated sine waves in time domain. To generate an appropriate cancellation signal, a digital cancellation system with a suitable topology and a proper algorithm has been proposed. For the best results, the algorithm's parametrization has been optimized by systematic investigations. Last, the system has been applied to a real PFC. The differential-mode EMI at 100 kHz has been actively suppressed by approximately 39 dB. As shown by systematic investigations, similar results can be expected for frequencies of up to at least 1 MHz. This cancellation system may also be applied to common-mode EMI by choosing appropriate configurations for the sensor, injector and decoupler.

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