Broadband Noise Suppression of Stationary Clocked DC/DC Converters by Injecting Synthesized and Synchronized Cancellation Signals

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Abstract—Active cancellation of disturbing signals is a common method in EMC of power electronic systems. In this paper, a new method of suppressing periodic disturbances is extended and applied. In this method, the disturbing harmonics are suppressed by a synthesized cancellation signal that is synchronized with the converter's operation. Here, the cancellation signal is synthesized from a number of destructive sine waves. The appropriate amplitudes and phases are found via a convenient and robust adaptive approach. As a special feature of this method, many troublesome effects, like delays or complex frequency characteristics, can be compensated easily. Therefore, this method does not suffer from the same limitations as previous active techniques. Until now, the method has only been proven for a small number of harmonics. In this work, it is applied to a wide frequency range of 150 kHz to 30 MHz of a 48 V/12 V DC/DC converter, e.g. for automotive applications. An optimization strategy is developed from a causal model of the system. A test setup is realized, and the sensor's and injector's performances are discussed regarding the automotive EMC standard CISPR 25. Measurement results for the artificial network and the antenna are presented. The additional power losses are estimated.

Keywords—Adaptive; Cancellation; Power Electronics; EMC; EMI; Harmonics

I. INTRODUCTION

Clocked systems, such as PWM power electronic converters, tend to be considerable sources of electromagnetic disturbances. To comply with the EMC standards (e.g. [1] in automotive), the disturbances are commonly reduced by applying passive filters or shields that may be bulky, heavy and expensive. Another strategy is the active cancellation of disturbing signals by a destructive interference between noise and anti-noise [2]. This strategy is applied commonly in acoustics and successively in EMC.

For EMC, active EMI filters have been introduced in [3] and elaborated on in [4], [5] and [6]. Like passive EMI filters, active filters are connected between the disturbance source and the sink. The disturbances are measured at the source (feedback type, Figure 1, a)) or the sink (feedforward type, Figure 1, b)), passed through a controller and injected back into the system in order to achieve a destructive interference between the signals. The possible structures of these active filters are further generalized and analyzed in [7] and [8]. As power electronic converters steadily gain significance, there are, amongst many others, investigations into DC/DC converters e.g. [9], motor inverters e.g. [10] and PFC systems e.g. [11]. Recently, comprehensive design guides have been developed for common mode [12], [13] and differential mode [14] active EMI filters. With the availability of fast FPGAs and DSPs, more complex digital (feedback type) active EMI filters have been developed and investigated for e.g. switch mode power supplies [15], photovoltaic dc-to-ac microinverters [16], DC/DC converters [17], [18] and arc welding inverters [19].



Figure 1: Cancellation types. a) Feedforward active filter, b) Feedback active filter, c) Cancellation by synthesized and synchronized waveforms

For a perfect cancellation of the signals, noise and anti-noise must be accurate opposites of each other and, therefore, exactly simultaneous. As the analog and/or digital signal processing of active filters causes an unavoidable delay, there are systematic limitations for the achievable reduction and the suppressible frequency range. This problem is analyzed in [20] and [21] for feedforward active filters. Measurements of a feedback active filter in [13] have shown a maximum achievable common mode suppression of approximately 20 dB at 1 MHz and a maximum frequency of approximately 8 MHz. Measurements of another feedback active filter in [14] have shown a differential mode suppression of 15 dB at 1 MHz and maximum frequency of approximately 3 MHz. As analytically shown in [19], also digital feedback implementations suffer from these unavoidable delay times. In experiments presented in [19], a delay time of merely 4.5 ns caused an instability of the digital active EMI filter worsening the system's EMI. Possible solutions for digital active EMI filters applied to stationary systems are depicted in [19] and realized in [18].

Another concept, Harmonics Cancellation (HC) has been shown first in [20]-[22]. Here, the disturbing harmonics are suppressed by a cancellation signal synthesized from synchronized sine waves (Figure 1, c)). Since the cancellation is based on an artificially synthesized signal that is synchronous to the system's EMI, the problems mentioned above are avoided. Delay times of the injection system can easily be compensated by phase-shifting the generated sine waves. For finding the parameters compensation signal Adapted Harmonics Cancellation (AHC) was developed in [20]-[22]. All bothersome effects, like delay times or frequency responses of the components, are compensated adaptively. By applying this method to stationary clocked systems, the effectivity of active noise suppression could be improved widely. In [20]-[22], the signal synthesizer and AHC have been implemented on a continuously adapting FPGA system (CAHC, Continuously Adapted Harmonics Cancellation) with A/D and D/A converters (ADC/DAC). In [21], EMI reductions of approximately 80 dB for single harmonics of up to 50 MHz have been achieved in a simplified demonstrator setup. In [20], the cancellation system has been applied to an automotive DC/DC converter. Six harmonics of the converter's disturbances have been suppressed below the class 5 limit of the standard CISPR 25 [1] in a frequency range of 150 kHz to 1.8 MHz. The cancellation signal was synthesized by six synchronized sinusoidal waveform generators and limited by the used digital signal processing algorithm.

In this work, a much wider frequency range of 150 kHz to 30 MHz could be suppressed by applying AHC and using a modified signal processing method. Since the disturbances are much wider than the necessary measurement bandwidth of 9 kHz, it is a broadband noise suppression method in regard to CISPR 25 [1]. This method, Previously Adapted Harmonics Cancellation (PAHC, introduced in [20]-[22]), is investigated in detail and successfully applied to a DC/DC converter. In this strategy, the cancellation parameters and/or waveforms are determined during a training process and stored in memory units. Since the adaption is done by an external trainer that is not required anymore after the training process, powerful hardware can be utilized for measuring (here: EMI receiver) and optimizing (here: PC). The cancellation system is reduced to the functionality of the signal synthesizer (here: arbitrary waveform generator or FPGA system) that either reads out a sampled waveform or internally synthesizes the cancellation waveforms from, e.g., frequency, amplitude and phase parameters. By doing so, the hardware expenses can be widely reduced in comparison to CAHC. Since such a system can easily suppress hundreds of harmonics, it is well applicable to a large frequency range.

At first, the methods HC, AHC and CAHC are briefly summarized, and PAHC is discussed in detail. For the training process of PAHC, an efficient and specialized optimization strategy is developed from a causal model of the system. Afterward, PAHC is applied to a stationary operating DC/DC converter in an automotive test setup. For the given test setup, the design of the injector is discussed. Furthermore, as a special feature of PAHC, the training is conducted for an actual noise sink, the artificial network. To do so, a test setup is realized containing an EMI receiver, a PC with Matlab for the control program, and an arbitrary waveform generator. To verify the method, the performance of the compensation structure and the cancellation waveform (found with the artificial network) are also evaluated with a rod antenna. The cancellation results are presented, and the power consumption of the cancellation system is discussed. Lastly, a practical realization example utilizing a FPGA system is presented. A conclusion closes the work.

II. ADAPTIVE STRATEGIES FOR ACTIVE HARMONICS CANCELLATION

In this chapter, Adapted Harmonics Cancellation (AHC) and Continuously Adapted Harmonics Cancellation (CAHC) are summarized. Afterward, the method Previously Adapted Harmonics Cancellation (PAHC) is introduced in detail.

A. Adapted Harmonics Cancellation (AHC)

The fundamental concept of AHC [20] is illustrated in Figure 2. The clocked system is the source of the disturbing harmonics that must be cancelled out. In this work, a DC/DC converter is considered as clocked system that creates harmonic disturbances due to the periodic switching of the transistors. The cancellation system is implemented on digital hardware and consists of an optimizer and a synthesizer. For cancellation, the synthesizer generates a sine wave for each disturbing harmonic. To find the right amplitudes and phases for the cancellation, an optimizer is utilized. The synchronicity of the generated sine waves and the disturbing harmonics is maintained by a suitable synchronization signal. To link the clocked system and the cancellation system, interfaces are necessary. A sensor is used to measure the disturbances that consists of an analog circuit and an ADC. To couple the cancelling waveform into the clocked system, an injector is necessary. This injector consists of an injecting circuit and a DAC.



Figure 2: Concept of Adapted Harmonics Cancellation (AHC)

B. Continuously Adapted Harmonics Cancellation (CAHC)

In CAHC, the cancellation signal is adapted during the operation of the clocked system. Therefore, all depicted elements must be placed within the overall device or system. In [20]-[22], this method has been realized on a programmable FPGA system with high-speed ADCs and DACs. A single-frequency adaptive notch filter has been implemented as a synthesizer, and the delayed LMS algorithm [23] has been applied as an optimizer.

C. Previously Adapted Harmonics Cancellation (PAHC)

For a reduction of the hardware requirements of the canceller, the concept of PAHC is introduced in Figure 3. In this strategy, there is an external trainer that teaches the canceller.



Figure 3: Concept of Previously Adapted Harmonics Cancellation (PAHC)

The device under test (DUT) consists of the clocked system (here the DC/DC converter), an injector, a synthesizer and a memory. Again, the clocked system is the source of EMI. The injector consists of an ADC and additional analog circuitry. In contrast to CAHC, there is an external trainer consisting of the sensor (e.g. EMI receiver with artificial network), an optimizer and an optional signal preprocessor. Naturally, the sensor must be well correlated to the emitted noise of the system. The trainer finds the optimal waveforms for cancellation and writes either completely sampled waveforms or parameter sets (amplitudes and phases) into the memory of the remaining system.

In a stand-alone operation, the optimized waveforms are synthesized using the previously found amplitudes and phases and passed to the injector. For synchronicity with the clocked system, a trigger signal is sent to the synthesizer. In power electronic systems, the control signals for the transistors are convenient signals for synchronization. Of course, the noise of the clocked system changes with the operating mode. For, e.g., power electronic systems, important parameters include the duty cycle, the input and output voltages, the transfer power and the temperature. In prior tests, for all relevant parameter variations, a respective anti-noise waveform must be found and stored in the memory. The information for the operating parameters is usually known by the controller of the clocked system and, therefore, available. This information is sent to and used by the synthesizer to select the optimum cancellation signal corresponding to the operating mode.

In this variant, the sensor and the optimizer are outsourced. Therefore, a minimized cancellation system can be realized. But, unlike CAHC, the cancellation signals are not continuously adapted. If there are changes in the system after training, the effectiveness of the cancellation may be reduced.

III. PARAMETRIZATION OF PAHC

In this chapter, a parametrization strategy for PAHC is presented. First, the optimization problem is depicted. Afterward, a causal model for the overall system is developed and analyzed. From this causal model, an identification procedure is derived that enables an easy calculation of the necessary cancellation parameters. The cancellation result is improved by an iterative application of the algorithm.

A. Optimization Problem

In this work, PAHC is demonstrated with an EMI receiver as the sensor's ADC. In general, PAHC must be trained for many different parameter combinations. To achieve reasonable training times, an efficient optimization strategy is crucial. In the case of an unknown system, there is the fundamental problem of a black box: For each harmonic k, there is a measurable residual disturbance level $Y_{res}(k)$ that depends on the complex amplitude $\overline{Y}_{anti}(k)$ that consists of the amplitude $Y_{anti}(k)$ and phase $\angle \overline{Y}_{anti}(k)$. There are essentially two strategies for optimizing such a black box: 1) Iterative search, or 2) Modelling and mathematical optimization. To quickly find the necessary parameters, the second option is pursued.

B. Modelling of the System

In Figure 4, a causal model for the overall system is presented. There is the noise (EMI) of the clocked system $\bar{Y}_{\rm EMI}(k)$ and the anti-EMI $\bar{Y}_{\rm anti}(k)$ that is synthesized by the canceller for the specific harmonic k. EMI and anti-EMI propagate through the overall system and interfere at every point. Here, for optimization purposes, the residual EMI $\bar{Y}_{\rm res}(k)$ at the sensor is of interest. Both for the EMI and the anti-EMI, respective transfer functions $\bar{H}_{\rm EMI}(k)$ and $\bar{H}_{\rm anti}(k)$ can be formulated that describe the propagation of the signals through the system.



Figure 4: Causal model

So, (1) follows for the residual EMI.

$$\overline{Y}_{\text{res}}(k) = \overline{H}_{\text{EMI}}(k) \cdot \overline{Y}_{\text{EMI}}(k) + \overline{H}_{\text{anti}}(k) \cdot \overline{Y}_{\text{anti}}(k)$$
(1)

To find the optimum parameters for the anti-EMI, it is not necessary to identify both $\overline{Y}_{\text{EMI}}(k)$ and $\overline{H}_{\text{EMI}}(k)$. To reduce the

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optimization problem, the disturbance $\bar{Y}'_{\rm EMI}(k)$ is considered at the sensor directly:

$$\bar{Y}_{\rm res}(k) = \bar{Y}'_{\rm EMI}(k) + \bar{H}_{\rm anti}(k) \cdot \bar{Y}_{\rm anti}(k)$$
(2)

By EMI receiver measurements, the absolute value of the residual noise $\bar{Y}_{res}(k)$ is detected:

$$Y_{\rm res}(k) = |\bar{Y}'_{\rm EMI}(k) + \bar{H}_{\rm anti}(k) \cdot \bar{Y}_{\rm anti}(k)|$$
(3)

The complex amplitudes can be separated into their amplitudes and phases:

$$Y_{\rm res}(k) = \left| Y_{\rm EMI}'(k) e^{j \angle \bar{Y}_{\rm EMI}'(k)} + H_{\rm anti}(k) e^{j \angle \bar{H}_{\rm anti}(k)} \right.$$

$$\left. \cdot Y_{\rm anti}(k) e^{j \angle \bar{Y}_{\rm anti}(k)} \right|$$
(4)

To reduce the number of unknown parameters, $e^{j \angle \bar{Y}_{EMI}^{\prime}(k)}$ is factored out, and $\angle \bar{H}_{anti}(k) - \angle \bar{Y}_{EMI}^{\prime}(k)$ is set to $\varphi_{diff}(k)$:

$$Y_{\text{res}}(k) = \underbrace{\left| e^{j \angle \bar{Y}'_{\text{EMI},k}} \right|}_{=1} \left| Y'_{\text{EMI}}(k) + H_{\text{anti}}(k) e^{j\varphi_{\text{diff}}(k)} \right|$$
(5)
$$\cdot Y_{\text{anti}}(k) e^{j \angle \bar{Y}_{\text{anti}}(k)} \right|$$

Now, the absolute value is calculated:

$$Y_{\text{res}}(k) = \left[\left(Y_{\text{EMI}}^{\prime 2}(k) + H_{\text{anti}}^{2}(k) Y_{\text{anti}}^{2}(k) + 2Y_{\text{EMI}}^{\prime}(k) H_{\text{anti}}(k) Y_{\text{anti}}(k) \right. \\ \left. \left. \cdot \cos\left(\angle \bar{Y}_{\text{anti}}(k) + \varphi_{\text{diff}}(k) \right) \right) \right]^{\frac{1}{2}}$$

$$(6)$$

For the theoretical optimum of $Y_{res}(k) = 0$, EMI and anti-EMI must have the exact same amplitude:

$$Y_{\text{anti,opt}}(k) = Y'_{\text{EMI}}(k) / H_{\text{anti}}(k)$$
(7)

and an inverted phase:

$$\angle \bar{Y}_{\text{anti,opt}}(k) = 180^{\circ} - \varphi_{\text{diff}}(k) \tag{8}$$

So, to find the optimum parameters for cancellation, $Y'_{\rm EMI}(k)$, $H_{\rm anti}(k)$ and $\varphi_{\rm diff}(k)$ must be identified.

C. Identification of the System's Parameters

In the following, a strategy is proposed to find the system's parameters that (ideally) requires only 4 measurements for each harmonic. If distortion is no issue in the signal generation and the overall system, the parameters for all harmonics can be found in parallel. In each step, the cancellation signal is synthesized by

$$y_{\text{anti}}(t) = \sum_{k=1}^{K} Y_{\text{anti}}(k) \cdot \cos(2\pi \cdot kf_0 \cdot t + \angle \bar{Y}_{\text{anti}}(k)) \quad (9)$$

Firstly, $H_{\text{anti}}(k)$ is identified. To do so, the clocked system is turned off $(Y'_{\text{EMI}}(k) = 0)$, and a test signal with arbitrary amplitudes $Y_{\text{anti,test}}(k)$ and arbitrary phases $\angle \overline{Y}_{\text{anti,test}}(k)$ is used. From (6), the following relationship results:

$$Y_{\text{res,meas.}}(k) = H_{\text{anti}}(k) \cdot Y_{\text{anti,test}}(k)$$
(10)

Since $Y_{\text{anti,test}}(k)$ is known and $Y_{\text{res,meas.}}(k)$ is measured, the transfer function $H_{\text{anti}}(k)$ can be calculated by

$$H_{\text{anti}}(k) = \frac{Y_{\text{res,meas}}(k)}{Y_{\text{anti test}}(k)}$$
(11)

Secondly, $Y'_{\rm EMI}(k)$ is identified. To do so, the canceller is turned off $(Y_{\rm anti,test}(k) = 0)$, and the disturbances of the system $Y_{\rm res,meas.}(k)$ are measured. In this case, the measured disturbance directly corresponds to $Y'_{\rm EMI}(k)$:

$$Y_{\text{res,meas.}}(k) = Y'_{\text{EMI}}(k) \tag{12}$$

The optimum cancellation amplitude $Y_{anti,opt}(k)$ can be calculated by (7). Note that the system's transfer functions may change when the clocked system (here the DC/DC converter) is turned on. For example, the inductance of inductors may change when they are biased by the DC current of the converter. To avoid this issue, the characterization measurement can be done at temperatures, currents and voltages similar to the values found during the system's normal operation.

Thirdly, $\varphi_{\text{diff}}(k)$ must be found. To identify the phase, the clocked system remains turned on, and test measurements $Y_{\text{res,meas.}}(k)$ are done with $Y_{\text{anti,opt}}(k)$ and different values $\angle \bar{Y}_{\text{anti,test}}(k)$. For identification, (13) is derived from (6) and (7). Note that $Y'_{\text{EMI,known}}(k)$ has been determined in the previous step of the algorithm.

$$\cos\left(\angle \bar{Y}_{\text{anti,test}}(k) + \varphi_{\text{diff}}(k)\right) = \frac{1}{2} \cdot \left(\frac{Y_{\text{res,meas.}}(k)}{Y'_{\text{EMI,known}}(k)}\right)^2 - 1$$
(13)

To find $\varphi_{\text{diff}}(k)$, the nonlinear problem of (13) is translated into a linear problem with two unknown parameters A(k) and B(k):

$$A(k)\sin\left(\angle \bar{Y}_{\text{anti,test}}(k)\right) + B(k)\cos\left(\angle \bar{Y}_{\text{anti,test}}(k)\right)$$
$$= \frac{1}{2} \cdot \left(\frac{Y_{\text{res,meas.}}(k)}{Y'_{\text{EMI,known}}(k)}\right)^2 - 1$$
(14)

As there are two unknown parameters, at least two test measurements must be done. For two test measurements, the following relationship results:

$$\begin{cases} \sin\left(\angle \bar{Y}_{\text{anti,test,1}}(k)\right) & \cos\left(\angle \bar{Y}_{\text{anti,test,1}}(k)\right) \\ \sin\left(\angle \bar{Y}_{\text{anti,test,2}}(k)\right) & \cos\left(\angle \bar{Y}_{\text{anti,test,2}}(k)\right) \end{bmatrix} \begin{pmatrix} A(k) \\ B(k) \end{pmatrix} \\ = \frac{1}{2 \cdot Y_{\text{EMI,known}}^{\prime 2}(k)} \begin{pmatrix} Y_{\text{res,meas,1}}^2(k) \\ Y_{\text{res,meas,2}}^2(k) \end{pmatrix} - 1 \end{cases}$$
(15)

Note that a difference of 180° between the two test phases leads to a singular, non-invertible matrix. It can be shown that the matrix is best conditioned for phase differences of 90°. After solving for A(k) and B(k), $\varphi_{\text{diff}}(k)$ is found by

$$\rho_{\rm diff}(k) = \operatorname{atan2}(-A(k), B(k)) \tag{16}$$

and the optimum phase for cancellation $\angle \bar{Y}_{\text{anti,opt}}(k)$ is calculated by (8).

Fourthly, the cancellation signal is synthesized from the optimum amplitudes $Y_{\text{anti,opt}}(k)$ and the optimum phases $\angle \overline{Y}_{\text{anti,opt}}(k)$.

D. Further Optimization by Additional Iterations

Theoretically, an ideal cancellation signal can be found by the following the four steps described above. In reality, the precision of the algorithm is limited by, e.g., distortion, measurement noise or nonlinearities. To further improve the EMI suppression, additional iterations can be done. The basic concept is to keep the cancellation signal and to find an additional cancellation signal that suppresses the residual disturbances. By doing so, the cancellation signal is successively improved until it meets the requirements or the hardware limits like the noise floor of the ADC. These additional iterations can be done by repeating steps 2 through 4 of the algorithm. After step 4, the old signal is optimized by superposing the new one.

IV. DEMONSTRATION

In this chapter, PAHC is demonstrated. The test setup is presented first. Then, the sensor is set. Afterward, an injector is selected and realized. Its passive attenuation is discussed, and the dynamic range of the DAC is adjusted by adding attenuators. The cancellation results are presented, and the power consumption is discussed. Finally, a practical realization of the cancellation system is presented.

A. Test Setup

The referenced test setup [1] is depicted in Figure 6. The clocked system is a 48 V/12 V DC/DC converter evaluation board (GS61008P-EVBBK) in a shielding enclosure with the necessary periphery. The switching half bridge is the noise source. An arbitrary waveform generator controls the DC/DC converter by a PWM signal with a switching frequency f_0 of 300 kHz and a constant duty cycle of 25 %. So, there will be disturbing harmonics with a spacing of 300 kHz. The arbitrary waveform generator is controlled remotely by a PC. The load is a 1 Ω resistor. The converter is connected to an artificial network by the supply line. Since there is only one supply line over the measurement copper table as ground plane, only differential mode disturbances must be considered. The artificial network is the noise sink that is used to find the optimum cancellation parameters. Its signal is measured by an EMI receiver and sent to a PC. The rod antenna is the secondary noise sink that is used to verify the found solution. For the antenna measurement, the test setup is placed in a shielded chamber. This signal is measured by a second EMI receiver. The power supply provides a constant voltage of 48 V. To demonstrate the proposed method and algorithm, the disturbances of the converter shall be suppressed in regard to the class 5 limit [1] in a frequency range from 150 kHz to 30 MHz. Due to the switching frequency of 300 kHz, there are 100 harmonics that must be suppressed. So, the cancellation signal is synthesized from 100 cancelling sine waves.



Figure 6: Photograph of the test setup

B. Sensor

The sensor is a critical component as it determines the achievable precision of the cancellation. As stated before, an artificial network is chosen as sensing circuit. In a practical application, there may be no artificial network but the actual network that offers no particular measurement port. In this case, a sensor must be applied before the teach-in process that can be removed afterward. Possible sensors include, e.g., current sensors or antennas. It would also be possible to build a sensing circuit and a measurement port into the DUT. The measurement and A/D-conversion are conducted by the EMI receiver R&S ESRP. A resolution bandwidth (RBW) of 9 kHz is used. Since the converter is operating stationary, the average and peak emissions are basically the same. In the following, the average emissions are considered due to their much stricter limit requirement. If the average emissions comply with the requirement, the peak emissions will comply with the limit as well. The disturbing spectrum and the noise floor of the sensor's ADC can be found in Figure 5. Furthermore, the class 5 limit of the CISPR 25 [1] is depicted that consists of segmented limits for longwave (LW, 150 kHz-300 kHz), mediumwave (MW, 530 kHz-1.8 MHz), shortwave (SW, 5.9 MHz-6.2 MHz) and cell broadcast (CB, 26 MHz-28 MHz). Note that there are no limits in between those bands. Obviously, the disturbing spectrum is far above the limit of class 5. Since the noise floor of the measurement is far below the given limit, the dynamic range of the sensor is sufficient. The signal-to-noise ratio (SNR) can be estimated by the difference between the highest measurable signal (fundamental wave at 300 kHz, 97 dBµV) and the noise floor (about -5 $dB\mu V$) to approximately 100 dB. Note that it is possible to adjust the attenuator, the preamp and also the resolution bandwidth during measurement to increase the dynamic range even further, as long as the transfer function of the sensor does not change.



C. Injector

1) Inductive vs. Capacitive Injection

The injector is implemented inside the DUT on the 48 V supply line. Since there are only differential mode disturbances, the injector only needs to inject a differential mode cancellation signal. For an injection, there are basically two fundamental strategies: 1) Inductive injection and 2) Capacitive injection. Due to the adaptive approach of AHC, there is no systematic limitation for the injection circuit as transfer functions are easily compensated via the amplitudes and phases of the cancellation signal. In [20]-[22], an inductive injector has been chosen. Since the whole line current flows through one winding, and the magnetizing inductance must be set very high to avoid high magnetizing currents, inductive injectors tend to be rather large [11]. These problems are avoided by capacitive solutions. So, a capacitive injector is realized in this work.

2) Design of the Injecting Circuit

In Figure 7, the schematic of the overall system is depicted. There is the power supply, the artificial network, the supply line, the converter and the load resistance. The residual voltage $Y_{res}(k)$ is measured by the EMI receiver at the artificial network and sent to the PC that is used as optimizer and signal processor according to the optimization strategy depicted in III. The signal generation is realized by the arbitrary waveform generator (AWG) Tektronix AFG3252 that generates the voltage $\overline{Y}_{anti}(k)$ with its internal resistance of 50 Ω . This AWG utilizes DACs with an effective analog bandwidth (-3 dB) of 225 MHz, a vertical resolution of 14 bits, and a voltage range of ±5 V. Due to the internal resistance of 50 Ω , a maximum current of 100 mA can be injected at maximum voltage of the AWG.

A coupling capacitor of 100 nF is the main part of the injecting circuit. The AWG basically injects a current that partially flows into the artificial network and the converter. Note that the cancellation must take effect at the sink. The current flowing into the converter is superfluous for the cancellation and should be minimized to reduce the power consumption of the cancellation system. So, it is necessary to evaluate the current divider between the noise sink and the converter. Due to the stabilizing capacitor, the converter has a very low input impedance Z_{conv} of approximately 1.1 Ω for 300 kHz. On the other hand, the impedance of the noise sink Z_{sink} (consisting of the impedance of the artificial network and the supply line) has a value of approximately 12.3 Ω at 300 kHz. Therefore, most of the injected current would flow into the converter and not support the cancellation. To fulfill the cancellation at the noise sink, a very high injected current would be necessary. To improve the circuit behavior, the high frequency input impedance of the converter can be increased by a decoupling inductance L_d . Here, an inductor with an inductance of 5.8 μ H has been chosen. The resulting input impedance of the decoupled converter Z_{dec} has a value of approximately 13.3 Ω at 300 kHz. Now, Z_{dec} is significantly larger than the original input impedance Z_{conv} . Therefore, a much larger portion of the injected current supports the cancellation at the noise sink. The impedance of the decoupling circuit can still be increased to improve the circuit's performance further. Since the supply line

and the decoupling inductance both show a reasonable impedance over 300 kHz, the matching can be assumed to be valid for frequencies of up to 30 MHz.



Figure 7: Schematic of the overall system

A photograph of the realized DUT is depicted in Figure 8. There is the DC/DC converter with an auxiliary supply for the transistors' driver and an external fan (below the converter). The control signal for the transistors is generated by the AWG and brought into the system through a BNC feedthrough. The injecting circuit is placed between the input of the DUT and the converter. The anti-noise is also generated by the AWG and brought into the system through a BNC feedthrough.



Figure 8: Photograph of the DUT

3) Passive Attenuation of the Injecting Circuit As the injector is an additional passive structure, it causes a passive attenuation of the disturbances. In Figure 9, the disturbances with and without the injecting circuit are depicted. To fulfill the limit, most of the noise suppression must be achieved by the active system.



Figure 9: Passive attenuation of the injecting circuit

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4) Adjustment of the Dynamic Range

Now, the dynamic range of the injector is investigated that is mainly governed by the resolution, and therefore the signal-tonoise ratio (SNR), of the DAC. As shown theoretically in [20] and experimentally in [21], the SNR of the DAC limits the achievable noise suppression independent of frequency. The only frequency limitation is given by the DAC's bandwidth. Note that the utilized AWG could potentially suppress a frequency range of up to 225 MHz which is the upper frequency limit of the device. To achieve the best cancellation results, all of the available SNR should be utilized. To adjust the dynamic range to the disturbances, an amplifier or an attenuator can be used in between the arbitrary waveform generator and the injecting circuit. In Figure 10, the transfer functions from the injector's DAC to the sensor's ADC are considered for different attenuators. Note that the transfer function is only determined for the harmonics indicated by the markers. Obviously, the transfer function is reduced by higher attenuations. In the following, the injector's boundaries are transferred to the sink with these transfer functions.



Figure 10: Transfer function for different attenuators

From (17), a signal-to-noise ratio (SNR) of approximately 86 dB follows for the DACs of the AWG with its voltage range of $V_{\text{DAC,max}} = \pm 5$ V and its quantization of $b_{\text{DAC}} = 14$ bits.

$$\Delta V_{\text{DAC,SNR}} = b_{\text{DAC}} \cdot 6.02 \, \text{dB} + 1.76 \, \text{dB}$$
(17)

The RMS value of the highest generable single sine wave may be calculated by (18). Here, a value of approximately 3.5 V (131 dBµV) results.

$$V_{\text{DAC,sine,max}} = |V_{\text{DAC,max}}| - 3 \text{ dB}$$
(18)

The resulting noise floor $V_{\text{DAC,NF}}$ can be calculated by (19). A value of approximately 45 dBµV results.

$$V_{\text{DAC,NF}} = V_{\text{DAC,sine,max}} - \Delta V_{\text{DAC,SNR}}$$
(19)

By considering the transfer function $H_{\text{anti}}(k)$, both, the noise floor and the highest generable sine wave can be transferred to the sink:

$$V_{\text{DAC,sine,max,sink}} = V_{\text{DAC,sine,max}} + H_{\text{anti}}(k)$$
 (20)

$$V_{\text{DAC,NF,sink}} = V_{\text{DAC,NF}} + H_{\text{anti}}(k)$$
(21)

For the different attenuators, these two boundaries are depicted in Figure 11. Furthermore, the limit of class 5 and the

envelope of the disturbances are plotted. The first consideration is the noise floor. Obviously, it should be below the limit line. This condition is met for all attenuators. Nevertheless, the noise floor of 0 dB is already close to the limit line. The best solution appears to be an attenuator of 20 dB. The second consideration is the highest generable sine wave. Clearly, the highest generable sine wave must be above the noise envelope. Otherwise, the necessary sine wave for cancellation could not be synthesized. For an attenuator of 20 dB, the highest generable sine wave for the fundamental wave is below the noise envelope. Therefore, this attenuator cannot be applied. A good solution is the attenuator of 10 dB for the given ADC with its dynamic range. Note that these considerations can also support the determination of the necessary number of bits for an ADC.



Figure 11: Injector's boundaries at the sink for different attenuators

In the synthesis, multiple sine waves are superposed creating a new signal that often has a higher maximum voltage than the individual sine waves. So, the time domain signal that is depicted in Figure 12 must be investigated. Note that the anti-EMI for a 20 dB attenuator is only an estimation as the necessary voltage range is too wide for the DAC. It can be seen that the voltage range of the DAC is best utilized for an attenuation of 10 dB. In the next step, the optimum attenuator Att_{opt} can be calculated by (22) from the maximum voltage range of the DAC $V_{DAC,max} = \pm 5$ V and the maximum absolute voltage of the synthesized signal $V_{synth,max}$ for an attenuator of 0 dB (here: 0.92 V).

$$Att_{\rm opt} = 20 \text{ dB} \cdot \log_{10} \left(\frac{|V_{\rm DAC,max}|}{V_{\rm synth,max}} \right)$$
(22)

An optimum attenuator of 14.7 dB follows. So, in further measurements, an attenuator of 13 dB is applied.



Figure 12: Anti-noise signal in time domain for different attenuators

Interestingly, in the time domain, the fundamental wave is very prominent. This is due to the fact that the fundamental wave's noise is the strongest and that the transfer function is at a low value. At approximately 0 and 0.8 μ s, the switching events of the transistors can be identified.

D. Cancellation Results

After the systematic design and adjustment of the sensor and the injector, the algorithm from III.C can be applied. The arbitrary waveform generator and the EMI receiver are controlled by a PC. The algorithm has been implemented in Matlab. According to III.D, three iterations of the algorithm are done. The measurement results for the artificial network and the rod antenna are presented in Figure 13 and Figure 14, respectively. In both cases, the requirement of class 5 is fulfilled. For the first harmonics, there are reductions of up to 56 dB for the artificial network. Even for 30 MHz, reductions of 30 dB could be achieved. Note that the precision of the cancellation is only limited by the technological boundaries that encompass, e.g, the injector's noise floor, the noise measurement precision and the linearity of the system.



Figure 13: Noise suppression at the artificial network



Figure 14: Noise suppression at the rod antenna

For the rod antenna, the noise suppression appears to be worse, but other effects are responsible for that. It can be assumed that the supply line's disturbances at the artificial network are, in fact, suppressed. However, the rod antenna as second sensor measures not only the E-field of the supply line but also of other structures (e.g. imperfect coaxial shields and shielding enclosure). Since the supply line's disturbances are suppressed, the other E-fields become dominant in the measurement. So, the measured E-field is higher than it would be for the supply line alone and the noise suppression appears worse than it actually is. Nevertheless, the measurement complies with the requirement of class 5 of CISPR 25.

Note that the found cancellation signal is only viable for the considered operating point of the converter. For operation at, e.g., other transfer powers or temperatures, respective cancellation signals must be selected.

E. Power Consumption

In the following, the power consumption of the active signal injection is estimated. In a worst-case scenario, the injector's DAC is constantly at its maximum voltage $V_{\text{DAC,max}} = \pm 5 \text{ V}$ and its termination impedance is 0 Ω . In this case, the injector's power is completely dissipated at its internal resistance R_{DAC} that is 50 Ω for the utilized arbitrary waveform generator. So, the maximum power of the injector can be calculated to $P_{\text{anti,max}} = (\pm 5 \text{ V})^2/50 \Omega = 500 \text{ mW by (23)}.$

$$P_{\rm anti,max} = \frac{V_{\rm DAC,max}^2}{R_{\rm DAC}}$$
(23)

To estimate the actual power consumption of the cancellation circuit, the cancellation signal $v_{anti}(t)$ found in IV.D is considered. The RMS value $V_{anti,rms}$ is calculated to approximately 2.39 W. Due to the attenuators applied in IV.C.4), there is an impedance matching between the AWG's internal resistance $R_{DAC} = 50 \Omega$ and its termination $R_{termination} = 50 \Omega$. So, the actual power consumption can be estimated to only 57 mW by (24). Considering the converter's transfer power of $(12 \text{ V})^2/1 \Omega = 144 \text{ W}$, the cancellation losses' share is below 0.04 %.

$$P_{\text{anti}} = \frac{V_{\text{anti,rms}}^2}{R_{\text{DAC}} + R_{\text{termination}}}$$
(24)

F. Exemplary Realization with FPGA system

In this section, an exemplary realization of the cancellation system is presented. For realization, a FPGA development system Red Pitaya STEMlab 125-14 is used. This system comprises a programmable FPGA and two high speed DACs with a sampling rate of 125 MS/s, a vertical resolution of 14 bits, and a maximum voltage range of ± 1 V. The output bandwidth of the development system is limited to 50 MHz. The built-in AWG application of the FPGA system is used to generate the control signal for the converter and the anti-noise for cancellation. So, the total cancellation system is placed inside of the shielding enclosure (Figure 15). To account for the smaller voltage range of the DACs, the attenuator introduced in IV.C.4) is reduced to 3 dB. The communication with the external trainer is realized via Ethernet.

In Figure 16, the measurement result is depicted. It has been found that the cancellation signal of the Red Pitaya (with the built-in AWG application) is not as clean and stable as the signal of the high-end AWG from Tektronix. Therefore, the system shows a slightly worse performance than the AWG over the total frequency range. Due to this issue, the class 5 limit is not achieved anymore. Nevertheless, there is a considerable noise suppression and the system complies at least with the class 4 limit [1]. Therefore, in practical realizations, special care must be taken for a clean signal generation to avoid any deviations.



Figure 15: Photograph of the DUT with FPGA system



Figure 16: Red Pitaya vs. AWG (at the artificial network)

V. CONCLUSION

In this work, Adapted Harmonics Cancellation (AHC) has been applied to a wide frequency range of a DC/DC converter's noise. Unlike active EMI filters, the cancellation signal is artificially synthesized and injected in synchronicity with the disturbing system. By doing so, bothersome delays can be completely eliminated that would otherwise limit the achievable noise suppression and the maximum frequency range. Here, a special method for finding the synthesized signal, Previously Adapted Harmonics Cancellation (PAHC), has been investigated. In this method, the cancellation signals are found by a trainer in prior tests and stored in the cancellation system. As a special feature, the training is done for the actual noise sink, an artificial network. To find the appropriate cancellation signal, an efficient parametrization strategy has been derived from a causal model of the overall system. A demonstrator setup has been realized to train the cancellation system with a PC. The performance of the sensor has been discussed, and an injector has been designed. Measurements with an arbitrary waveform generator as cancellation system prove that the disturbances at both the artificial network and the rod antenna are suppressed regarding the class 5 limit of CISPR 25 in the frequency range of 150 kHz to 30 MHz. The fundamental wave of 300 kHz has been suppressed by nearly 50 dB and even the higher harmonics

of up to 30 MHz have been reduced by over 30 dB. It has been shown that the injector only consumes a marginal amount of power compared to the transfer power of the converter, namely less than 0.04 %. Finally, a practical realization with a FPGA and D/A converter has been presented that complies with the class 4 limit of CISPR 25 in the frequency range of 150 kHz to 30 MHz.

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