A Combined Time and Frequency Domain Characterization Method for Modeling of Overvoltage Protection Elements

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***Abstract*—Nonlinear voltage sensitive protection elements, e.g. Multi-Layer Varistor (MLV) or Transient Voltage Suppressor (TVS) are useful to protect IC pins from ESD on System Level. Such elements might exhibit a significant voltage overshoot for fast transients. This work describes a combined time and frequency domain characterization method and its application to an MLV. Impedance measurements with VNA at different DC-bias points are used for model identification and parameterization. The static nonlinear IV-behavior of nonlinear model part at higher voltages and currents is extrapolated with a TLP IV-curve. The model is successfully validated with ESD pulses in time domain. The transient behavior including the occurring voltage overshoot can be reproduced with high accuracy.**

Keywords— Overvoltage Protection; Electro Static Discharge (ESD); ESD modeling; ESD simulation; Multi-Layer Varistor (MLV); Transient Voltage Suppressor (TVS)

I. INTRODUCTION

Overvoltages such as Electrostatic Discharges (ESD) are a serious threat to automotive, industrial, and consumer electronics. Discharge currents caused by a human or a tool can reach sensitive IC pins and damage the IC severely. Different strategies and design rules are available to system designers in order to avoid ESD failures on system level. A commonly used method is to provide an alternative ESD current path using an additional ESD shunt element. Nonlinear voltage sensitive protection elements, e.g. Multi-Layer Varistor (MLV) or Transient Voltage Suppressor (TVS) are useful to protect IC pins dealing with high bitrates. The selection of an appropriate protection element for a system can be a time-consuming trial and error optimization process. In addition, expensive hardware is required. Due to these problems, simulation-based ESD-optimization approaches are very attractive.

In the idealized case, the protection elements are considered as open circuit below the breakdown voltage. Above this voltage, the resistance drops rapidly to an approximately constant value. In [1] and [2], general characterization and modeling processes were presented, wherein the static high voltage IV-behavior is captured with a Transmission Line Pulser (TLP). The static characteristic is extended by a constant shunt capacitance modeling the parasitic capacitive behavior of the semi-conductor. In addition, a series inductance represents the terminal inductivity. However, some protection elements exhibit an overshooting fast transient response, as it is shown in Fig. 1 exemplarily for the voltage step response of MLV and TVS. The voltage overshoot could initiate the triggering of internal IC-protection structures and cause a system failure. Thus, a virtual system ESD optimization has to consider the turn-on effects.

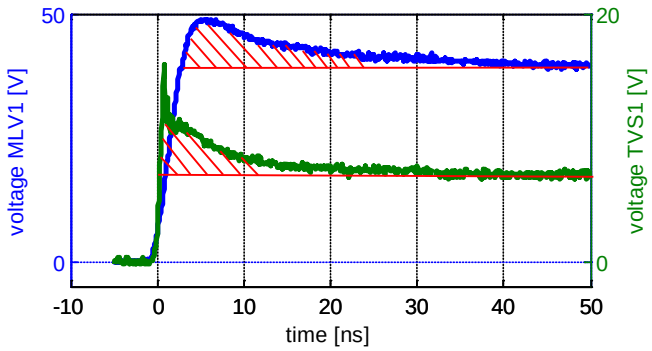

Fig. 1. Measured voltage overshoot for a MLV and TVS for a 100 V TLP pulse with 1 ns rise time

For power diodes the voltage overshoot is well known as forward recovery and modeling methods are presented e.g. in [3]. The authors in [4] apply the modeling method to TVS. Parameters are extracted by approximating TLP measurement data, no details about fitting are presented. Voltage overshoot of ZnO, as a key material of MLV, was analyzed in time domain on metal oxide surge arresters for high voltage application in [5]. The authors assume that at grain boundaries of the ZnO ceramic a potential barrier is built up and the dynamic behavior of the charge carriers on the potential barrier determines the turn-on process. However, no quantitative explanation of the effect could be found in literature. A SPICE based model for ZnO surge arresters is proposed by IEEE group 3.4.11 [6]. Parameterization of the model is done with time domain measurements. The authors in [7] present a study of DC-biased MLV in frequency domain. The method is suitable only for low currents due to thermal stress of the element. A rise in impedance before capacitive cut-off frequency is measured. The rise is supposed to be responsible

for a voltage overshoot in time domain. Consideration of nonlinear elements in both time and frequency domain is presented in [8]. The authors characterize a light emitting diode with impedance spectroscopy at different operating points. The results are used for model parameterization. The concept is proved by comparing time domain simulation and measurement for square pulse excitation with different repetition frequencies. However, only the capacitance of the diode was considered as voltage dependent.

This manuscript combines time and frequency domain characterization methods for more precise modeling of nonlinear ESD protection elements. Small signal impedance analysis at several operating points provides detailed information up to breakdown voltage region. The results are used to identify and parameterize a lumped element simulation model. The behavior of nonlinear model parts at high voltages and currents is extrapolated with static IV-curve. The method is applied to a MLV of type EPCOS CT0603K14G.

II. Characterization

A. *Frequency Domain*

For the investigation of the MLV impedance frequency response, a PCB is designed for VNA measurements. The Agilent Network Analyzer E5061B supports DC-bias up to 40 V and 100 mA. A series through 2-port configuration is selected [9], because of higher dynamic range compared to a reflection measurement (Fig. 2). MLV impedance Z_{MLV} is calculated with S-parameters using the formula

$$Z_{MLV} = 100\Omega \cdot \left(\frac{1 - S_{21}}{S_{21}}\right), \qquad (1)$$

wherein the 100 Ω refer to the sum of transmitter and receiver 50 Ω impedances. Frequency range from 10 kHz to 1 GHz is covered. A -10 dBm power level reduces distortion due to nonlinearity. The setup is carefully calibrated and the effects of SMA jack and PCB traces are de-embedded in a post process. Degradation of the MLV due to DC currents in form of a slight shift of the IV-curve is reported in [7]. The characterization with decreasing bias gains highest degradation in the first measurement and ensures similar degradation degree of the MLV at low bias levels. The measurement procedure is automated and controlled with MATLAB programming environment.

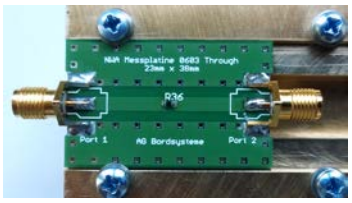

Fig. 2. Characterization PCB for impedance analysis under DC-Bias

Fig. 3 shows measured MLV impedance. Although 0.5 V steps are used in the measurements, only selected curves are included for better readability.

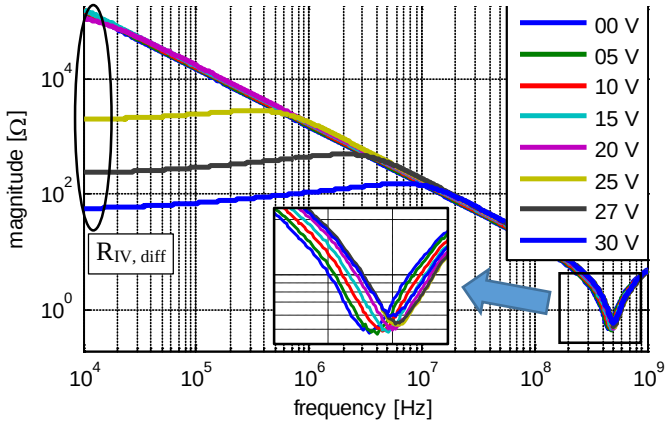

Fig. 3. Impedance Z_{MLV} of the MLV

As expected, the impedance of the MLV at low frequencies decreases with growing DC bias. This behavior complies with the IV-curve. However, the impedance exhibits additional increase before the cut-off frequency determined by capacitance of the MLV. Phase of the impedance becomes positive indicating inductive properties. The curves have their maxima at several MHz, which is conform to the voltage overshoot of MLV at about 20 ns measured in time domain (Fig. 1). In addition, an obvious shift of the resonance peak and the corner frequency to higher frequencies is observed indicating e.g. a decrease in element capacitance.

B. *IV-Curve*

The IV-curve describes the static behavior of the protection element up to several amperes. In device characterization for ESD modeling, the low current characteristic is commonly measured with a source meter unit (SMU, Keithley 2400) and high current with a transmission line pulser (HPPI-TLP/VF-TLP/HMM Test System TLP-3010C) [2]. The relation between these measurement results and VNA frequency response is established with IV-curves. For that purpose, the low current IV-curve is measured with the VNA. The resistive part of the impedance ($R_{IV,diff}$) at low frequencies is used (c.f. Fig. 3). Since only the small signal differential impedance is measured with VNA for each DC-bias voltage, a further processing of the data is required. Due to the series connection, the DC-bias (V_{VNA}) is divided between MLV, 50 Ω transmitter, and 50 Ω receiver resistances. A numeric integration over DC-bias provides the IV-curve of the overall setup

$$I_{MLV}(V_0) = \int_0^{V_0} \frac{1}{R_{IV,diff}(V_{VNA}) + 50\Omega + 50\Omega}\, dV_{VNA}. \qquad (2)$$

Due to the series connection, the MLV voltage (V_{MLV}) is the difference of DC-bias and voltage drop across transmitter and receiver

$$V_{MLV} = V_{VNA} - I_{MLV} \cdot 100\Omega. \qquad (3)$$

Fig. 4 confirms that there is a good agreement between VNA and SMU measurements. The static TLP results reflect the trend of the low voltage measurements. In addition, the

modeled IV-curve is included in this chart and is described in next section.

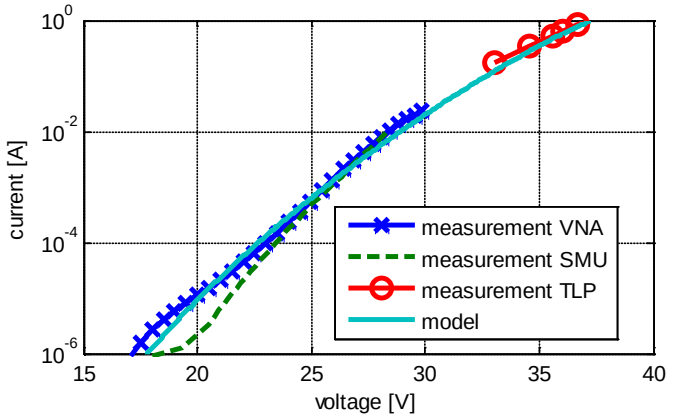

Fig. 4. IV-curve of the MLV, $I_{MLV}(V_{MLV})$

III. Modeling and Parameter Extraction

For the general structure of the proposed model, a simple behavior-based approach taken from [2] is used. This model consists of a parallel circuit of nonlinear resistor representing the static IV-curve and frequency characteristic at zero DC-bias modeled with a linear inductor and capacitor. The model is extended with a turn-on element in series to the IV-curve similar to [7] and [3]. The authors in [7] assume skin effect as the reason for overshoot. A skin effect resistance is added which can be realized by a truncated ladder network wherein its accuracy depends on the number of stages. In the simplest but numerically more stable case, it includes only a resistor in parallel to inductor. A MLV consists of multiple ZnO-grains connected in parallel and in series. Every set of two grains build a micro varistor. Thus, it is a legitimate assumption that the current through the device is proportional to the number of active micro varistors. This consideration implies that the values of turn-on elements should vary with current. Assuming skin effect as the reason for the observed turn-on behavior, the effects should be smaller for high currents. For the purpose of illustration, MLV can be compared to a stranded wire composed of several small gauge wires wherein the number of active wires is a function of current. Hence, the capacitance of the MLV is a sum of the package capacitance due to its layered structure and the capacitance on grain boundaries, which is a function of the applied voltage. While the described phenomena are physically located on grain boundaries, the elements R_0 and L_0 are attributed to a grain and should not change with voltage or current. R_0, L_0, and C_0 are present at high frequencies. R_0 is present at high currents as it will be shown in section III.A. In Fig. 5 the resulting model and designated nonlinear elements are shown. It should be noted that the inductance and resistance of the turn-on element depend on the overall current through MLV.

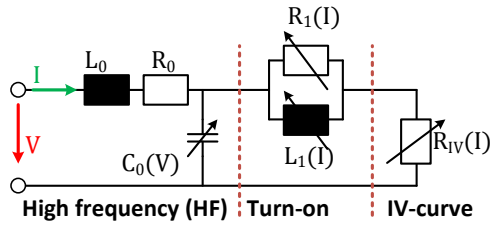

Fig. 5. MLV model including high frequency characteristic, turn-on circuitry and the static IV-curve

The model parameters for every DC-bias are determined by means of least-squares fit of the model impedance to the VNA measurements. Fig. 6 compares the results for 30 V. High frequency region is approximated with high accuracy. Due to mentioned simplifications, the model in Fig. 5 is not capable of totally reflecting the measurements in the turn-on region. However, a rise in impedance of same magnitude and frequency range is achieved.

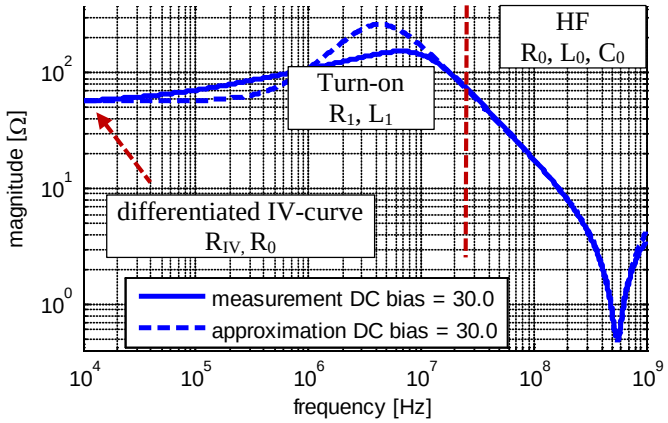

Fig. 6. Approximation of the measurement with model from Fig. 5

A. IV-Curve

With respect to proposed model in Fig. 5 the static behavior is established with a series circuit of bulk resistor R_0 and nonlinear resistor R_{IV}, which is approximated with MLV equation.

$$I = \left(\frac{V_{RIV}}{V_{1A}}\right)^n, \qquad I = \frac{V_{R0}}{R_0}, \qquad V = V_{R0} + V_{RIV},$$
$$\Rightarrow V = V_{1A} \cdot I^{\frac{1}{n}} + R_0 \cdot I, \tag{4}$$

where V_{1A} is voltage at 1 A and n varistor exponent. The intention of our approach is to predict the ESD behavior at high currents by VNA measurement at low currents. Therefore, the model parameters in (4) are fitted to measurement results considering full operating range. Deviations at low currents are accepted for the benefit of more precise approximation at high currents. Nevertheless, a good match at all relevant regions is achieved (c.f. Fig. 4).

B. *Turn-on Region*

Turn-on elements of the model depend on the overall current through MLV. VNA measurement provides only the DC-bias applied to the overall constellation. The operating point for every VNA measurement in terms of MLV voltage and current does not coincide with used DC bias in VNA. It is calculated by means of matching the measured and modeled differential resistance in static state. Modeled differential resistance is a derivative of (4):

$$R_{DC,diff} = \frac{dV}{dI} = \frac{d\left(V_{1A} \cdot I^{\frac{1}{n}} + R_0 \cdot I\right)}{dI} = \frac{V_{1A}}{n} \cdot I^{\frac{1-n}{n}} + R_0 \qquad (5)$$

For the turn-on elements an inverse proportionality with respect to MLV current has been expected. For high current all micro-varistors are active and the quantities should saturate to a particular minimum. With the same assumption for low current a maximum value representing the behavior of only one micro varistor is assumed. Measurement results are approximated with the following equations:

$$R_1(I_{MLV}) = \frac{1}{cR1 \cdot I_{MLV} + 1/R_{1,Max}} + R_{1,Min}$$
$$L_1(I_{MLV}) = \frac{1}{cL1 \cdot I_{MLV} + 1/L_{1,Max}} + L_{1,Min} \qquad (6)$$

where cR1, cL1 are the proportionality factors. Constants $R_{1,Max}$, L_{1Max}, $R_{1,Min}$, L_{1Min} provide maximum and minimum values for both functions respectively. Fig. 7 shows approximation results of the measurement. Equations (6) are evaluated for current up to 20 A.

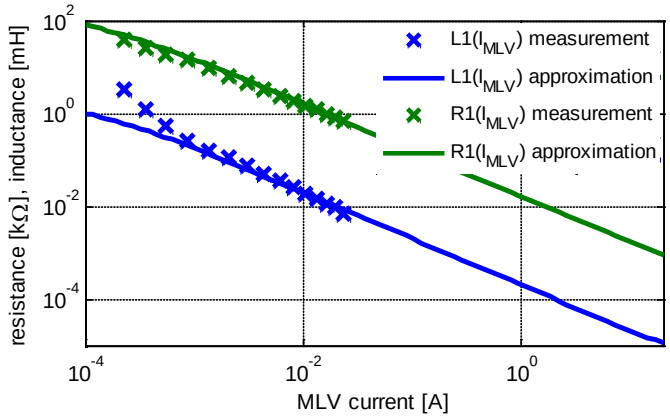

Fig. 7. Turn-on elements versus MLV current

C. *High Frequency Region*

Bulk resistance R_0 and series inductance L_0 are measured constant at different DC biases apart from some noise.

Microscopically, every two ZnO grains form two junctions placed back to back with each other. Its capacitance is proportional to square root of the applied voltage [12]:

$$C \approx \frac{1}{\sqrt{V_{MLV}}} \qquad (7)$$

Macroscopically, the layered MLV structure comply with a multi-layer ceramic capacitor with ZnO acting as dielectric. Biased with voltage below breakdown, the ZnO ceramic can undergo polarization. Both effects overlap to the overall MLV capacitance. In measurement, a linear decrease of the capacitance with MLV voltage is observed up to breakdown region (c.f. Fig. 8). At 27 V capacitance has its minimum of approx. 80 % of the nominal value. Hereafter a slight increase is noticed. This movement cannot be explained with (7). However, after the breakdown voltage the conductive parts of the MLV will dominate the overall behavior. Therefore, capacitance is approximated with a second order polynomial.

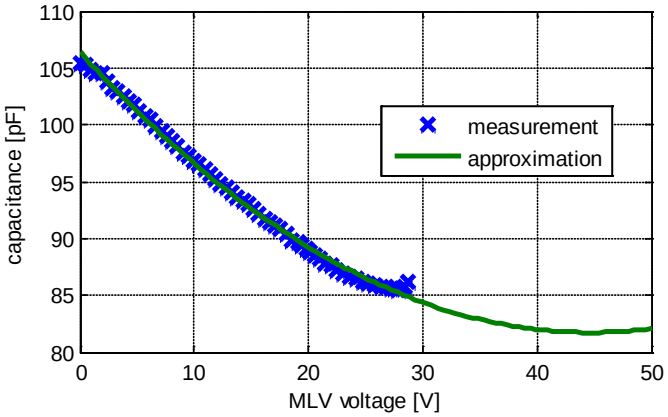

Fig. 8. Capacitance versus MLV voltage

D. *Implementation in VHDL-AMS*

The static IV-curve and nonlinear capacitance can be implemented in many electronic circuit simulators with support of equation defined blocks. Implementation of the nonlinear turn-on element is challenging, because of the parallel circuit (see Fig. 5).

```
architecture improved of MLV is
  quantity vTurnOn across iL1, iR1 through node1 to
node2;
  quantity vMLV across iMLV through node2 to node3;
  quantity L1, R1: REAL;
  .. --------------------------
  .. -- other quantities
  .. --------------------------
begin
  .. --------------------------
  .. -- High Frequency Elements
  .. --------------------------
  iMLV == (vMLV/V1A)**N;-- IV-curve
  L1 == 1.0/(cL1*iMLV+1.0/L1Max)+L1Min;-- nonlinear
inductor
  R1 == 1.0/(cR1*iMLV+1.0/R1Max)+R1Min;-- nonlinear
resistor
  vTurnOn == L1*iL1'dot;
  vTurnOn == R1*iR1;
end architecture improved;
```

Fig. 9. VHDL-AMS code for the IV-curve and turn-on part of the MLV

The current through each branch (iL1 and iR1) is only a fraction of the overall MLV current (iMLV) and a straight forward implementation of the function in III, B is not possible. Such problems can be handled with VHDL-AMS. Free quantities (L1 and R1) are defined for turn-on resistance and inductance connected to node1 and node2. The values are functions of the overall MLV current (iMLV between node2 and node3). These quantities are used for calculation of the relationship between voltage overshoot (vTurnOn) and branch currents (iL1 and iR1). Fig. 9 shows VHDL-AMS code section for IV-curve and nonlinear turn-on element. The code for high frequency part is cut.

IV. Simulation Results

A TLP measurement is used for model verification. The used TLP produces rectangular pulses with 1.1 ns rise time. TLP measurement setup was modeled and model was verified in former projects [10]. For demonstration purposes the simple MLV model according to [2] is also simulated. Results for a 100 V TLP pulse are shown in Fig. 10 and Fig. 11.

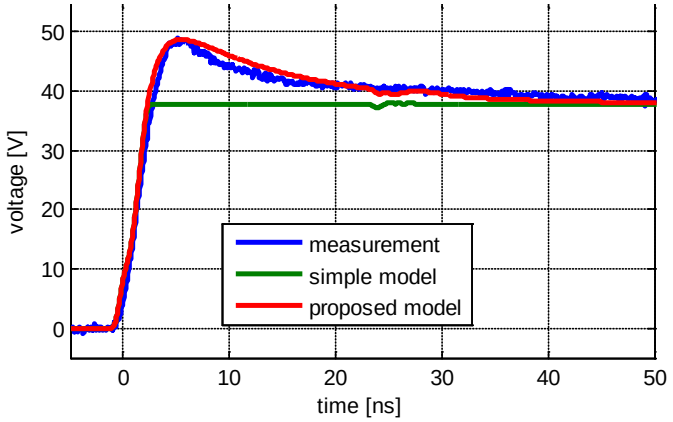

Fig. 10. Simulated and measured voltage for 100 V TLP pulse, proposed model (red), former simple model (green)

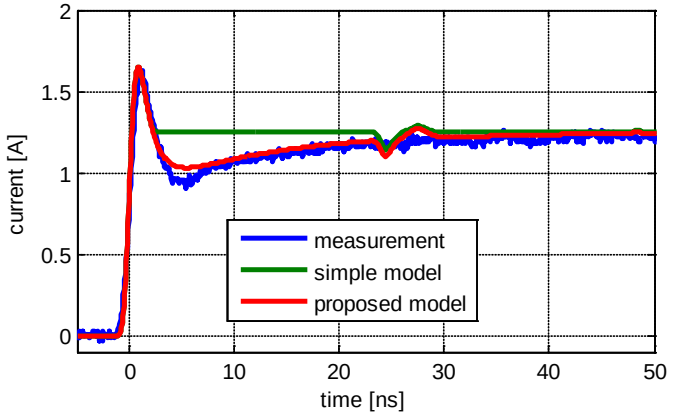

Fig. 11. Simulated and measured current for 100 V TLP pulse, proposed model (red), former simple model (green)

A voltage of 36 V is measured in saturated state. The over shoot of 48 V is around 33 % higher. Simulated waveforms with simple model goes immediately over to the static state. In contrast to the simple model, the presented model precisely predict the magnitude of the voltage overshoot. Simulated voltage and current accurately follow the measurement.

An additional verification is done by means of NoiseKen generator compliant to the IEC 61000-4-2 standard. In comparison to a TLP discharge, the double exponential IEC waveform is more complex and has a considerably higher initial peak. The model for a NoiseKen generator was presented and verified by measurements with different low and high-ohmic loads in [11]. MLV acting as ESD protection element is loaded with IEC ESD pulses. The setup in Fig. 12 is used. Clamping voltage of the protection element is measured with a scope over a serial 1 kΩ resistor and a 12 dB attenuator.

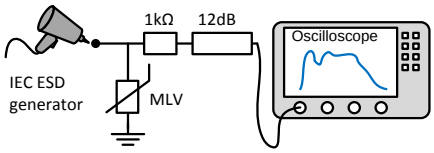

Fig. 12. Measurement and simulation setup for IEC ESD pulses

The proposed model predicts the clamping voltage with high accuracy (c.f. Fig. 13). Unexpectedly, the clamping voltage after 40 ns of the proposed model is lower than of the simple model. This trend is continuing up to ca. 200 ns. The reason is the decreasing IEC current, which cause a negative voltage drop over the turn-on element.

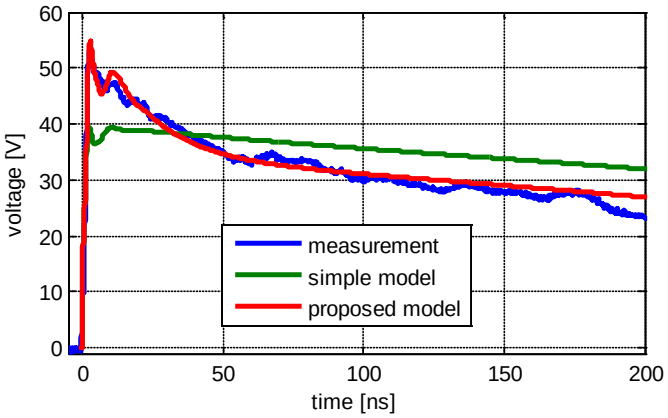

Fig. 13. Simulated and measured voltage for 1 kV IEC 61000-4-2 ESD, proposed model (red), former simple model (green)

V. Conclusions

Numerical simulation-based optimization approaches for overvoltage immunity are very attractive and require accurate models for nonlinear voltage sensitive protection elements. MLV and TVS experience turn-on effects for fast transients and a significant voltage overshoot were analyzed. In this paper, a combined time and frequency domain characterization method and its application to a MLV was presented. Nonlinear properties of the MLV were identified, modeled and parameterized using impedance measurement with VNA at different DC-bias points. The behavior of nonlinear model parts at higher TLP voltages was extrapolated with a static IV-curve. The model was successfully validated with TLP and ESD pulses in time domain. Voltage overshoot was reproduced

with high accuracy. Moreover, the method can also be applied to other high voltage pulses, e.g. burst and surge.

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