Simulation of ESD Thermal Failures and Protection Strategies on System Level

Stanislav Scheier, Friedrich zur Nieden**, Bastian Arndt*, Stephan Frei

***Abstract*—In this paper approaches for the modeling and simulation of thermal destruction of ICs due to ESD are discussed from a system point of view. Considered systems consist of ESD generator, PCB, protection element, and IC. A direct connection between the ESD generator and the system is always assumed. For the modeling of IC ESD destruction, the electric behavior model of an IC pin to ground or supply is extended with a thermal destruction model. The thermal model consist mainly of a thermal resistance and a thermal capacitance. When structure temperature reaches a threshold a failure is assumed. All needed model parameters can be found with a set of measurements and tests. No internal knowledge of the IC or protection element structures is required.**

The methodology was applied to several ICs, protection elements, and system structures with emphasis on automotive electronics. All needed component model parameters were generated from measurements. Models and parameter measurements are described. Results from system simulation were compared to system test results with hardware. In most cases the simulation could predict well the destruction behavior of a system. Thermal failure and Safe Operating Area (SOA) prediction quality are compared. The described simulation method helps with selection of protection strategies and optimization of system ESD robustness.

***Index Terms*— electrostatic discharge (ESD), system level ESD, thermal destruction/failure criterion, SOA, overvoltage destruction/failure, overcurrent destruction/failure**

I. Introduction

A low ESD-robustness of electronic systems might cause failures during manufacturing or operation. Appropriate test methods are available in order to find during the development process whether ESD protection is sufficient for an intended application or not [1], [2]. The ISO ESD-test standard for automotive electronic control units (ECU) demands for direct contact discharge testing of all connector pins, which might lead to an extremely time consuming test of up to hundred and more pins. When an electronic component/system fails a test, normally the robustness is increased in a time consuming and expensive trial and error process. Expert knowledge is needed to select promising protection improvements. The complex interaction between many system components makes the prediction of a protection performance very difficult. Several design rule sets were developed in the past and can be found in [3], but the complexity of the problem makes rule application difficult and success is not guaranteed. Due to the aforementioned problems numerical simulation-based ESD-optimization approaches are very attractive. The trial and error optimization process can be accelerated and hardware that might be expensive (and in prototype status) is not required.

For any part of the system a modeling and calculation strategy is required. A good summary of available approaches can be found in [3], [4], and [5]. Consideration of the complete system requires a unified simulation methodology. A semiconductor consortium described in [6] the "System Efficient ESD Design (SEED)" process where several modeling ideas are combined for system simulation. Here, mainly the electric behavior of the system is considered. However, one of the major challenges is to define pass/fail criteria. SEED assumes a failure when the Safe Operating Area (SOA) (in terms of overcurrent and overvoltage) is left. As a common approach, the SOA current threshold is defined as the maximum current an IC clamping structure can stand and the maximum allowed voltage level depends on the manufacturing technology. As robustness thresholds depend always on the test pulse duration and shape, which can vary in a wide range due to system structures, prediction quality might be low.

Some authors reported on the application of the SEED process. In [7] the ESD behavior of two products is simulated. The proposed IC-pin and protection element models are purely static. Failure of an IC-pin is considered by the residual current amplitudes at the first and second peak of the IEC pulse which are related to CDM and TLP measurements. Oscillations due to the PCB might make the analysis of the robustness difficult due to many current peaks. In [8] an USB2 interface on a signal processing board is investigated. Common mode ferrites (CMF) are analyzed in detail, nonlinear effects of CMF are demonstrated and modeled. Also here residual voltage and current amplitudes are used as failure criterion. [9] shows a study on a headphone pin for mobile applications. A TVS model is extended with self-heating and forward recovery. The authors could achieve a good match between measured and simulated currents through

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the pin. However, no failure model for the pin is proposed. Other authors [10] simulated a system consisting of an inverter and some passive components. IBIS data is combined with measured TLP data for modeling. The IC-internal ESD protection structure is identified with respect to V_{dd}- and V_{cc}-pins. It is proposed to use the breakdown voltage of the output driver as failure criteria. An implementation of snap-back elements with a state machine is presented in [11]. In contrast to previous publications [12] shows characterization of the on-chip ESD clamps on wafer instead of packaged IC. The second residual current peak of HMM is used here for failure indication. All mentioned approaches can predict in some cases quite well failures but partially deviations are high. This might be caused by the complex current and voltage shapes induced through the system components. Strong ringing effects and short but high voltage or current peaks with low total energy content might cause SOA criterion to fail.

In [13] the system level ESD failure was modeled as a mixed electro-thermal problem, assuming that a significant portion of the failures is caused finally by thermal overstress. The destroyed region is assumed to be overheated by the flown electric current, which is a common assumption for semiconductor destruction modeling. Overheating was detected using Wunsch-Bell approach [14]. The application only to a single IC pin is shown here and accuracy of this example might not be high enough for system design.

In this paper a system simulation methodology mainly applicable for virtual packaging and handling sensitivity classification of unpowered electronic modules (e.g. ISO 10605 [2]) is presented and systematically applied to a large set of IC-pins, protection elements, and PCB structures. Thermal failures are assumed and modeled using thermal RC circuits. Simulation focus is based mainly on an estimation of maximum structure temperature and less on prediction of the voltage and current amplitudes. Due to this assumption some simplifications in system modeling process are applicable and the modeling and parametrization process for all involved components is presented. No detailed information about internal structure of components or the manufacturing process is required, which makes the approach useful for practical application.

The paper has the following structure. Section II explains the simulation approach and the developed models of individual system components. In section III the simulation and measurement results are compared for example configurations, and the thermal failure criterion is validated. Additional examples for useful configurations are analyzed in section IV using the simulation. Section V discusses the main advantages of the proposed method.

II. Modeling and Simulation of ESD System Test Setups

A. Simulation Approaches

A simulation-based ESD robustness evaluation requires that a large and complex test setup must be reproduced in a simulation model with sufficient accuracy. Different simulation methods are possible, leading to different modeling approaches.

3D structure simulation can be seen as the most general method for devices (e.g. [15]) and complex setups, but demands for many constructive details and material parameters will result in a time-consuming modeling procedure. Models often require long computation times or might become numerically unstable. Considering only the destructive ESD current and voltages, circuit models for Kirchhoff laws-based network simulators like SPICE or VHDL-AMS [16], taking into account the integral behavior of system elements, can reduce calculation efforts or at first enable the simulation of larger systems. As an ESD system test simulation might require not only the currents and voltages, but also the heat flow and temperatures in an IC, the problem must be understood as mixed electro-thermal, assuming that a significant portion of the failures is caused by thermal overstress. Such problems can be well-treated with mixed-domain simulators based on modern modeling languages like VHDL-AMS.

B. Structured System Model

Simulation of a system using linked component models with defined interfaces is a straight forward approach. In Fig. 1 the simulation block model for an ESD current injection test setup is shown. It consists of several independent models which are arranged according to the current flow.

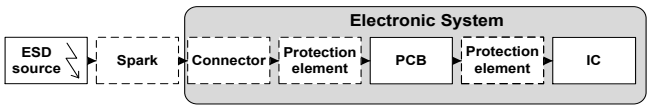

Fig. 1: Simulation setup consisting of circuit modules

In many cases it is sufficient for an accurate system model to consider only the ESD pulse source, the transmission path, and the pulse sink. More elements, shown in Fig. 1 with dashed boxes, can be added when the influence of the system connector cannot be neglected or ESD protection elements should be considered. For the simulation of air discharge a spark model might also be needed. As many tests are conducted in the contact discharge mode and connectors are often small, both component models are of less importance and are not discussed further here.

The quality of a system simulation mostly depends on the accuracy of each single component model. In the next section approaches for modeling ESD system test components for thermal based failure prediction are discussed.

C. Component Models

1) Pulse Generators Models

Pulse generators are used to specify the ESD robustness of electronic systems. Not only the standardized IEC 61000-4-2 or the ISO 10605 generators, but also Transmission Line Pulsers can be used for pre-compliance analysis.

a) IEC 61000-4-2 or ISO 10605 ESD Generator

IEC and ISO ESD generators are very similar due to harmonized specifications. The ISO standard demands a

higher maximum charge voltage and additional discharge network values. One simulation model for both standards is sufficient.

In an ESD generator, a defined RC network is discharged which is responsible for a pulse in current waveform. Furthermore, the structure of the generator and the relay are discharged. The discharge of these parts results in a very narrow pulse, superimposing the RC network pulse. This pulse is defined in the standards only by the rise time and the amplitude. Two parallel RLC circuits with pre-charged capacitors can be sufficient for a basic ESD generator model [17]. The simulation results shown here are based on such a model.

For more accurate models a consideration of constructive details is necessary. Due to missing specifications in the standards, several realizations of ESD generators are available on the market, complying with the standardized current curve, but having different electrical behavior under changing load conditions, especially at higher frequencies. Depending on the discharge load, deviations of up to 70% between the peak current amplitude, could be measured for comparing several generators complying with the IEC standard [18]. For a realistic system ESD simulation, a model should reflect the large variations between the different ESD generators. A compilation of available modeling approaches is given in [3].

b) Transmission Line Pulser Models

A transmission line pulser (TLP) [19] is mainly dominated by the discharge of a charged transmission line and can be modeled straightforward with a transmission line and linear circuit element models. The line is discharged via a relay which can be considered as an ideal switch. The rising and falling edges can be controlled by rise time filters, modeled with lumped elements.

2) Printed Circuit Board Structures

The current injected by the ESD generator into a system is conducted through a PCB structure to the ICs. Modeling the PCB current transmission behavior can be understood as a typical signal integrity (SI) or power integrity (PI) problem. A large amount of research was done in this field and many different modeling approaches are available. In general the more accurate the models, the higher the modeling and computational costs. A good overview of the state of the art in SI/PI-modeling can be found e.g. in [21].

The solutions can be separated into circuit (or transmission) line theory-based and full wave-based. The latter, more complex method, requires detailed layout data which considers vias, coupling, and edge effects in the design. Here as full wave approach the Partial Element Equivalent Circuit (PEEC) method [22] is used in some examples. Comparisons have shown that influence of higher accuracy of this approach compared to transmission line based modeling is negligible for thermal based failure simulation. Transmission line model parameters can be found from analytic calculations, here formulas from [23] and [24] are applied. Also online calculators e.g. from [25] can help with modeling.

3) System Level ESD Protection

Several protection strategies on the system level are available. Some of them attenuate the ESD current and/or bypass it through non-critical paths on the PCB. Other methods try to avoid a discharge by an enclosure or special PCB design. Here only PCB current-shunt approaches are considered, which can be subdivided into frequency-selective and voltage-selective protection.

a) Frequency Selective ESD Protection Elements

Capacitors can be seen as important circuit elements for frequency-selective filtering. In many applications, like automotive PCBs, capacitors, often MLCC (Multi-Layer Ceramic Capacitor), are used in combination with the PCB trace inductance as LC low pass filter, bypassing the high frequency ESD-pulse to the ground. In spite of an operation of simple MLCCs out of the specification range, this solution can be seen in automotive electronics as a kind of standard. The capacitance of MLCCs is voltage-dependent and becomes smaller with increasing voltage levels such as ESD events. Also a dielectric breakdown may be triggered by ESD and causes failure on the system level. For an ESD protection simulation model this behavior must be considered. A modeling and time domain parameterization methodology of the high voltage behavior of MLCCs was published in [26]. The proposed model is used here and shown in Fig. 2 a).

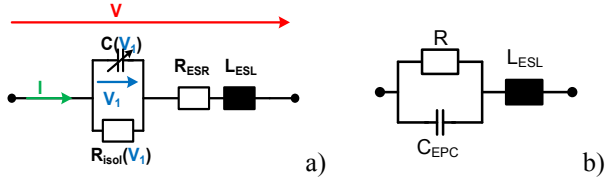

Fig. 2: Advanced equivalent circuit model of a MLCC (left), SMD resistor model (right)

Furthermore, current limiting SMD resistors are used, sometimes in combination with capacitors, and can be modeled at higher frequencies by adding a parallel capacitance and series inductance to a resistance as shown in Fig. 2 b). In automotive electronics only seldom ferrites or inductors can be found as ESD-protection and are not treated here.

b) Nonlinear Voltage Sensitive ESD Protection Elements

Typical voltage sensitive ESD protection elements are diodes, multi-layer varistors (MLV), voltage variable polymers (VVP), or spark-gaps. The latter both exhibit a high breakdown voltage and often a statistical behavior making the application for ESD protection difficult. Diodes or MLVs are quite reliable in their clamping behavior and the clamping voltages can also be low enough to protect sensitive electronics. Due to this reason only diode and MLV models are discussed here.

A variety of modeling approaches for nonlinear protection elements was published in the past. For most cases a model can be composed from a dynamic, memory containing linear part and a memory-less nonlinear part. The structured circuit and the principle of the modeling process are shown in Fig. 3. It is assumed here that the device is available for measurements.

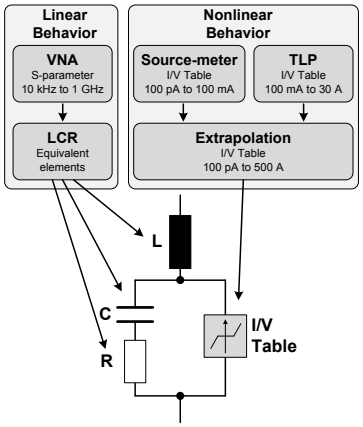

Fig. 3: Model structure and necessary measurements for model creation for nonlinear protection elements

(1) Nonlinear Memory-less Behavior Modeling

A nonlinear memory-less behavior can be modeled with a nonlinear resistor represented by an I/V curve. In Berkeley SPICE such elements can be modeled with mathematical functions [28]. However, it is very difficult to find a function describing the nonlinear behavior over several current decades without causing numerical problems. As many newer circuit simulators support the direct use of lookup-tables, a modeling concept which processes directly measured tabular data for the nonlinear, discrete protection element models is used here.

I/V measurements for low currents can be done using a source-meter-unit (SMU). A static measurement with higher currents would affect the components (due to thermal stress), therefore a TLP [29] is used. Both measurements are combined to a single IV curve. Linear extrapolation of the I/V characteristics can enlarge the simulation model application range.

Care has to be taken when the so called “snap-back diodes” must be considered. Here, an additional voltage dependent switch with hysteresis can be used as shown later.

(2) Linear Dynamic Behavior Modeling

The linear frequency-dependent behavior can be modeled with an RLC serial circuit. The impedance can be determined by measurements in the frequency domain using a vector network analyzer with low input power. RLC values can be found from the impedance curve, as shown in Fig. 4.

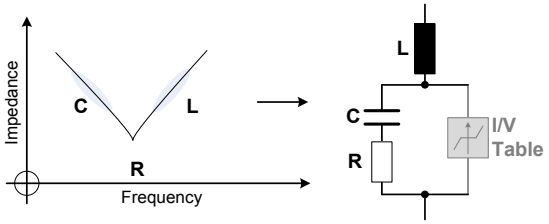

Fig. 4: Determination of equivalent models from a transfer function

4) IC Model

IC ESD current paths can be very difficult to predict due to complex and nonlinear structures. Full transistor level ESD modeling is possible only in special cases. Anyway, general failure behavior can be separated in thermal failures caused by longer current pulses and overvoltage failures triggered by high voltage pulses with some minimum energy content. Even without knowledge of the internal details behavioral models can be found. In this paper a practical approach based on simple measurements and testing is presented. It is assumed that the IC is physically available for measurements and tests. An electric model reproducing the pin voltage and current during a discharge is necessary. For the assumed thermal failure, a thermal behavioral model must be added. Both model parts are described here.

a) Electric Model

The electric behavior of an IC input can be modeled with a circuit as it is shown in Fig. 5. The model can be divided into two symmetric parts connected either to the ground or to the supply. Each of them consists of two or three (when snap-back effects have to be taken into account) behavioral descriptions.

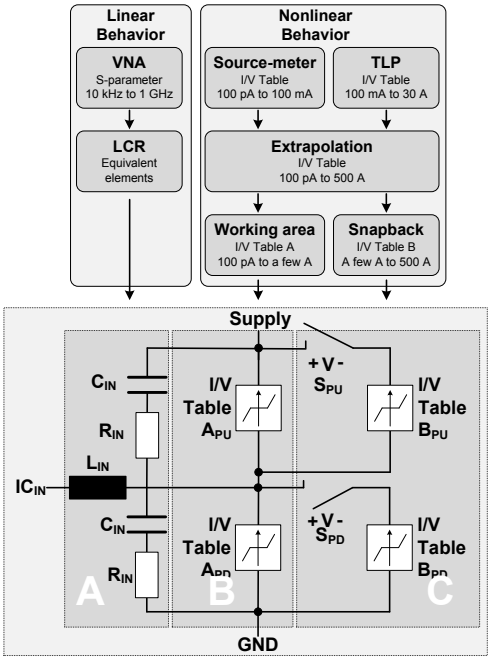

Fig. 5: Model structure and necessary measurements for model creation for IC input electric behavior

Block A of the model represents the frequency-dependent characteristic of the IC-pin with RLC components. Similar to the characterization of nonlinear protection elements, linear frequency-dependent behavior is measured with a VNA with low power excitation (voltage is far below the diffusion voltage). The measured impedance covers several parts of the IC, e.g. bonding wires, package, and die input structures. Direct mapping of measured results to the physical structures of the IC is not required. The capacitance of the device depends on the applied voltage, which creates additional nonlinearity. Here this influence is neglected.

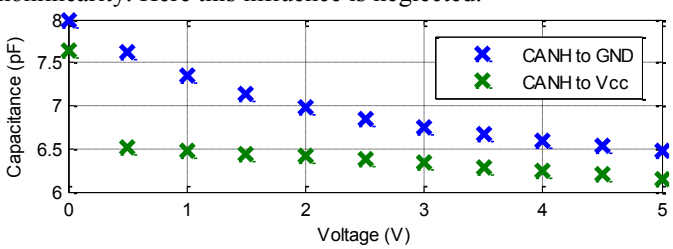

Fig. 6: Determination of equivalent models from a transfer function

Fig. 6 shows the capacitance of a CANH pin with respect to Vcc and to GND within normal operating range. The changes over the measured voltage range are less than 20 %.

As thermal failure is assumed here, the simple circuit shown in Fig. 5 (A) is sufficient for IC package modeling. When very high frequency behavior must be considered highly accurate approaches can be found e.g. in [35].

Block B and block C of Fig. 5 describe the static nonlinear behavior of the input structure. The model intends to reflect the current and voltage behavior until destruction of the component appears and is independent of the used technology or implementation. The nonlinear properties of the component are provided by I/V as explained above. In most applications, large capacitors are connected on the PCB between supply pins and ground. These provide an ESD current path with very low impedance. Consequently, in an unpowered setup, the on-chip current paths to ground and supply pins can be seen for an ESD event as connected and the upper and lower circuit in Fig. 5 are connected in parallel. Depending on the on-chip protection strategy one path might dominate the overall high current behavior. This means, the both current paths can be treated together in a failure model and substituted by a single RLC circuit in parallel with a single nonlinear resistors and, when snap-back must be taken into account, a switch with a second nonlinear resistor. A similar approach was proposed in [30] or [31] for overvoltage and overcurrent failure description based on the defined SOA.

b) Thermal Failure Model

ESD current can take different paths on the IC. Here a dominant IC structure carrying most of the ESD current is assumed. The current carrying part of the semiconductor is expected to melt at a certain temperature, which causes finally the damage to the IC [32], [33]. The heating process of the IC structure for ESD current pulses depends mainly on the heat power flow into and out of the threatened silicon region. This region has some thermal mass, represented by a thermal capacitance. The heat dissipation out of the threatened silicon region can be modeled with a thermal resistor [34]. Fig. 7 shows the extension of the electric behavior model with the thermal network. The heat power flow is calculated from the voltage and the current applied to the IC structure.

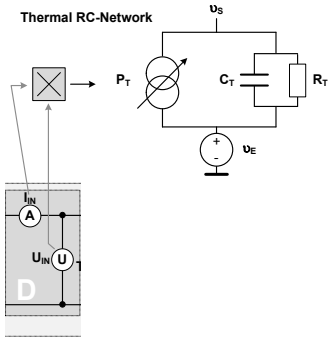

Fig. 7: General electro-thermal model

The problem here is the lack of information on the thermal capacitance C_T and thermal resistance R_T of the structure. Furthermore, the maximum allowed temperature ϑ_f is usually not known. This means three parameters of the behavioral model must be found. TLP-measurements can help finding the missing thermal network parameters. For a quasi-rectangular TLP excitation with the pulse width T_f and power amplitude P_f of the equivalent circuit in Fig. 7 the following temperature function can be derived:

$$\vartheta(t) = P_f\, R_T \left(1 - e^{-\frac{t}{R_T C_T}} + \left(e^{-\frac{t-T_f}{R_T C_T}} - 1\right)\Gamma(t - T_f)\right) \tag{1}$$

$\Gamma(t)$ is the step function. It is assumed here that the injected power is constant during the pulse width, i.e. R_T, and C_T are independent from temperature. Three regions can be separated:

1. Adiabatic region ($T_f \ll R_T C_T$): Here, no heat conduction through the structure is assumed. This can be true for the first ns. Thermal resistance can be neglected here and C_T can be calculated with:

$$\vartheta_f = \frac{P_f\, T_f}{C_T} \quad or \quad P_f = \frac{\vartheta_f\, C_T}{T_f} \rightarrow C_T = \frac{P_f\, T_f}{\vartheta_f} \tag{2}$$

2. Transition region: Here, heat conduction cannot be neglected any more, thermal capacitance and thermal resistance are active together. Failure power can be calculated with:

$$P_f = \frac{\vartheta_f / R_T}{1 - e^{-\frac{T_f}{R_T C_T}}} \tag{3}$$

3. Static region $T_f \gg R_T C_T$: For very long pulses as the static state can be assumed, here thermal capacitance can be neglected and R_T can be calculated here:

$$\vartheta_f = P_f R_T \text{ or } P_f = \frac{\vartheta_f}{R_T} \rightarrow R_T = \frac{\vartheta_f}{P_f} \tag{4}$$

As failure temperature and thermal resistance are not known and in (3) only the quotient is given, it is impossible to find both from measurement data. An estimation for the temperature is required. The melting temperature of silicon of 1683 K might be used. But not only silicon melting can cause a failure. In literature temperatures down to 900 K are reported to be responsible for failures [33]. Here, this minimum failure temperature ϑ_f of 900 K is assumed. When measurements were done only in the transition region, R_T and C_T can then be found by using two measurement points with formula (3) or finding a best power function fit to all measured failure energies vs. the TLP-pulse widths. A different value for ϑ_f will only result in different values for the assumed thermal capacitance and resistance, but the failure level will remain unchanged.

Fig. 8 shows the relation between destruction power and the applied TLP pulse width for the LIN IC. Here, different R_T and C_T combinations are shown exemplarily. A good match can be found with R_T=22 K/W and C_T=6 nJ/K. An

environmental temperature of 293 K is assumed. Using (2) and (4) with 25 ns and 200 ns TLP pulse width would give R_T=18 K/W and C_T=6 nJ/K.

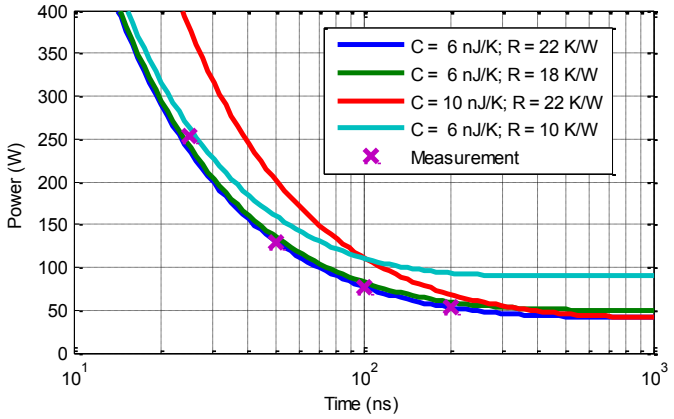

Fig. 8: Calculated and measured failure pulse power for a LIN IC (ATA6662C) for different TLP pulse width for four thermal RC network parameter sets and 900 K assumed as critical temperature

Finding $P_f(T_f)$ means, IC failure must be detected reliably. Detailed knowledge on functions and complex tests are required for larger ICs. As such complex functional can often not be realized in test facilities, leakage current measurements are used instead for failure detection. For a system with multiple ICs along the ESD current path a failure can be localized in some cases using the TDR technique [36]. Nevertheless, there is no guarantee that functional failures appear together with a change of the leakage current. In order to check the leakage current approach for a µC-GPIO pin the leakage current was measured and a simple functional test of the data receiving and transmitting capabilities was done after ESD testing. It could be found that the receiver mode of the GPIO-µC was first destroyed by an ESD. Measurement of the leakage current indicated a failure at the same voltage level. There is no guarantee for a correlation for all investigated pins and functions, but for the validation of a simulation methodology the leakage current test can be assumed to be sufficient. Fig. 9 shows an example with a CAN interface IC (TLE6250). The leakage current of the device was measured after different ESD generator discharges. The leakage current increases significantly after a 6.5 kV discharge. The component can be considered as damaged.

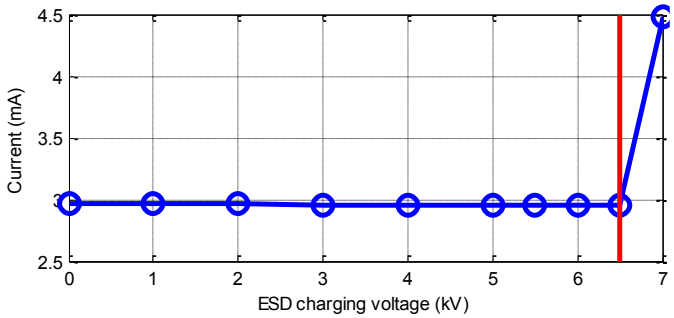

Fig. 9: Leakage current change at 40 V after ESD system level stress

D. Examples for Parameterized Component Models

The component modeling and parameterization methodology was applied to several protection elements and IC-pins. A model library together with an online-simulator was created and is available in Internet [27].

IC failure behavior depends strongly on possible current return paths and IC current paths vary with application, finding of a general characterization environment is difficult. All possible applications cannot be considered with a single test PCB. However, in data sheets or application notes, provided by the IC manufacturer, information on typical application circuits and recommended external components is given. Such typical application circuits were used on the test PCBs investigated in this chapter, not used pins were left open.

For showing the benefits of the above presented modeling approach, a transient voltage suppressor diode (TVS) and a multi-layer varistor (MLV) as external protection elements and two IC pins, a global pin of a CAN transceiver (CANH) and a GPIO-pin of an 8 bit microcontroller were used. Only the dominant current paths are considered here for further simulations. In Fig. 10 the measured IV curves of the devices are shown.

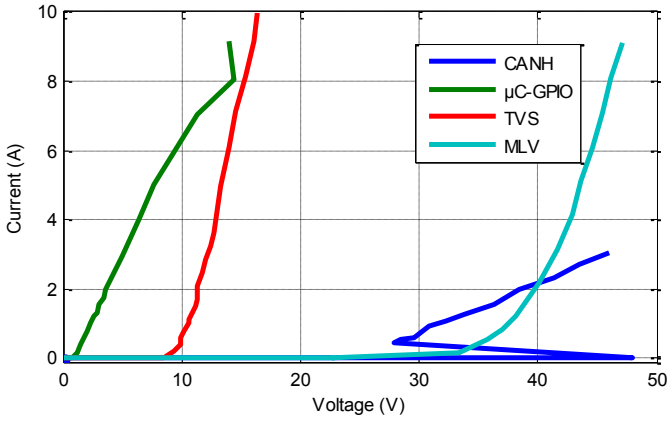

Fig. 10: Measured IV-curves for different devices, integration time 60-80 ns

For the SOA definition, in terms of overvoltage and overcurrent, as proposed by SEED, the current and voltage capability of internal structures is evaluated only for TLP with a fixed pulse width setting. The SOA values are derived from the TLP discharge measurement with the maximum charge voltage before IC failure. The TLP rise time is set to 1 ns and complies with the specification in IEC standard The major energy contribution of the IEC waveform is within the first 100 ns. This value is set for TLP pulse width. Derived SOA for the studied devices in terms of overvoltage and overcurrent are shown in Table 1.

The dissipated energy in Table 1 is calculated from measured voltage and current. This value strongly depends on the discharge waveform, e.g. failure energy for 200 ns and 100 ns settings are different.

Table 1: Failure levels for 100 ns TLP discharge for studied DUTs

	V_{Charge}	SOA	E_{crit}
Infineon µC XC866, GPIO-Pin	450 V	32 V/ 9 A	13.2 µJ
NXP CAN TJA1041, CANH-Pin	250 V	52 V/ 4 A	19.2 µJ

For a dielectric breakdown failure the critical TLP charging voltage should stay nearly constant for short pulses with different pulse width. As, in our measurements the critical TLP charging voltage dropped with increasing pulse width, the failure energy became larger with increasing pulse width. This indicates overheating failures. For dielectric breakdown failure detection very short TLP pulses with less than 25 ns pulse width might be required.

In Fig. 11, measured and simulated currents and voltages for a 100 V, 100 ns TLP discharge are shown. A significant part of the voltage overshoot for CANH and MLV, which can be observed during the first nanoseconds of the pulse, cannot be completely explained by package properties. The switching process is dominated by individual internal device properties, which are not yet modeled accurately, using the basic model structure described above. In the case of the µC-GPIO pin, the inductance of the socket used here has a significant impact on the voltage overshoot. Good matching of simulation and measurement is obtained after some nanoseconds. For the simulation of thermal failures, the influence of the first switching region can be neglected.

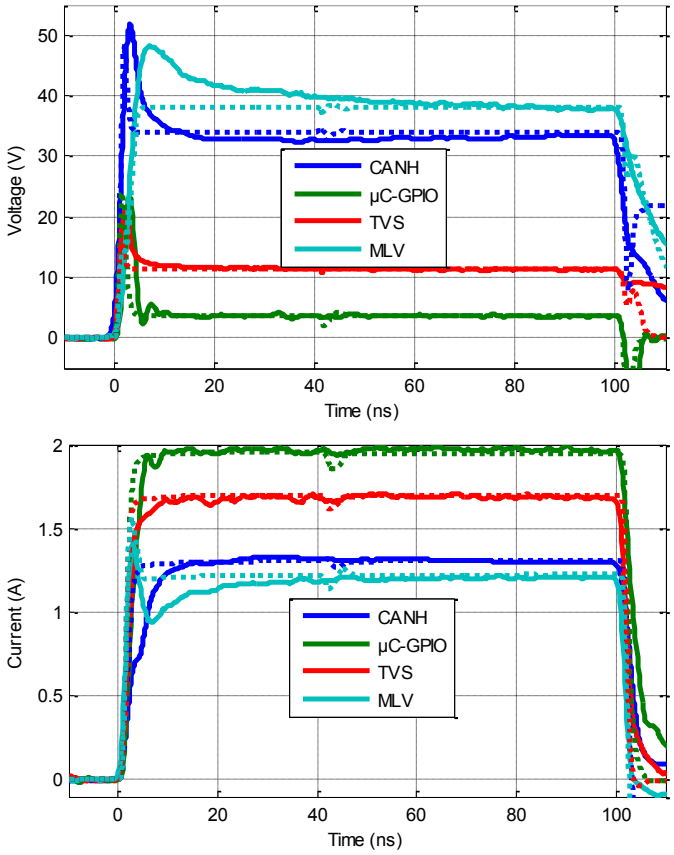

Fig. 11: Measured (solid line) and simulated (dotted line) voltage and current for TLP pulses of 100 V and 100 ns

III. ESD System Simulation

In this section the proposed modeling and simulation methods are applied to different devices and circuits. More examples are shown in order to describe the advantages of the approach. While some applications are described in detail, a summary of other results is presented in diagrams.

A. Validation Method

Simulation results are compared to measurements. Each configuration was stressed with a NoiseKen (TC815-R) ESD generator, which is compliant to the IEC 61000-4-2 standard. Three discharges within 3 seconds were applied for a particular charge voltage level. The leakage current of the tested devices were measured using an SMU at two voltage amplitudes before changing the discharge voltage level. If no significant change of the leakage value was observed in comparison to the last measurement, the generator charge voltage was increased in steps of 0.5 kV or 1 kV. All IC failure levels were tested with a minimum of 2 ICs. Current measurements were done using a Tektronix CT-1 current probe and a LeCroy 6 GHz oscilloscope in the setup shown in Fig. 12.

B. Simulation of IC Failures - Comparison to Measurement

Several PCB configurations without and with external protection devices were investigated. Simulation results are compared to measurements to verify the simulation approach.

1) Configurations without System Level ESD Protection

The validity of TLP-characterized IC failure models is verified by using an IEC ESD generator to compare the measurement and simulation results. Table 2 shows the measured and the simulated charge voltage levels. The simulated and measured current waveforms at the destruction voltage level applied to the µC-GPIO pin are shown in Fig. 13. The results show that the thermal failure models may accurately simulate the IEC ESD robustness.

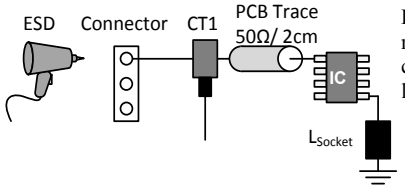

Fig. 12: Simulation and measurement setup for configurations without system level ESD protection

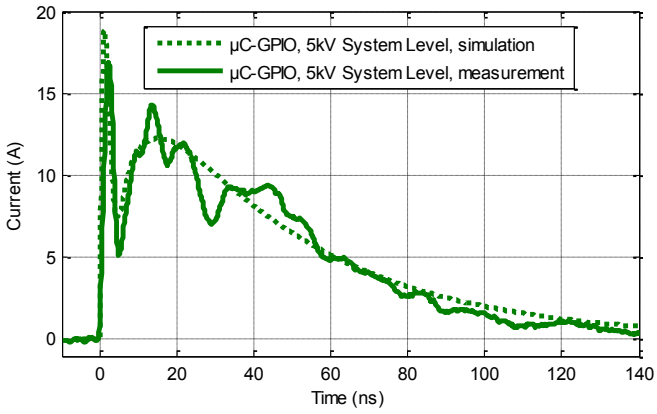

Fig. 13: Simulation and measured current for µC-GPIO through the connector of the characterization PCB

Table 2: Measured and simulated IEC robustness on demonstrator PCB

DUT	$V_{ESD, SIM}$	$V_{ESD, MEAS}$	Deviation
Infineon µC XC866, GPIO-Pin	5.0 kV	5.5 kV	+10 %
NXP CAN TJA1041, CANH-Pin	2.4 kV	2.5 kV	+4 %

Several ICs were characterized simulated and tested regarding IEC ESD robustness to verify the thermal failure modeling approach. Results are shown in Fig. 14. The highest deviation could be observed for an Atmel LIN transceiver (ATA6620), where the measured IEC robustness is 50 % higher. Deviation between measurement and simulation is less than 10 % for all of the other IC-pins.

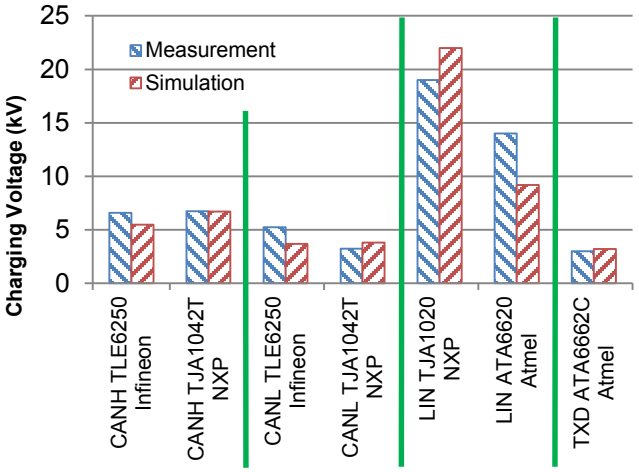

Fig. 14: Measured and simulated robustness on the system level in different configurations

2) Configurations Including a Nonlinear Protection Element

The IEC ESD failure levels of IC input pins with protection elements (PE) were measured on a more complex PCB. In the following example PCB parameters were taken from an automotive control unit. The protection element is placed parallel to the connector pin, which is separated by a 10 cm PCB trace from an IC as shown in Fig. 15. The PCB trace was modeled with transmission lines and parameterized as described in section II. The ESD current was measured between the PE and IC input.

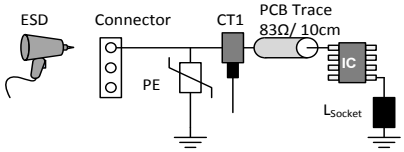

Fig. 15: Measurement and simulation setup for configurations including nonlinear protection elements

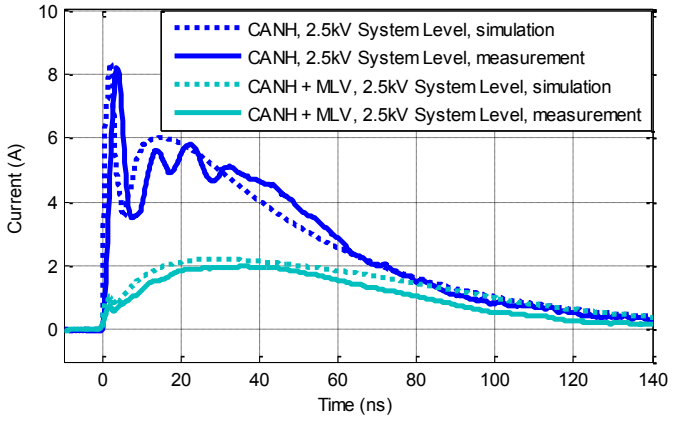

Fig. 16: Simulated and measured currents through the TJA1041T CANH-pin for 2.5 kV charging voltage with a MLV

In Fig. 16 the measured and simulated waveforms are compared for configurations with and without an MLV. The measured curves are similar to the simulation results. Although, the MLV has a lower breakdown voltage, the setup allows triggering of the internal protection of the CANH-pin. The residual ESD generator pulse at the CANH-input can be predicted accurately by the simulation model.

In Fig. 17 the effectiveness of various protection elements in different systems is shown. The IEC robustness level can be predicted with high accuracy by using the thermal failure model.

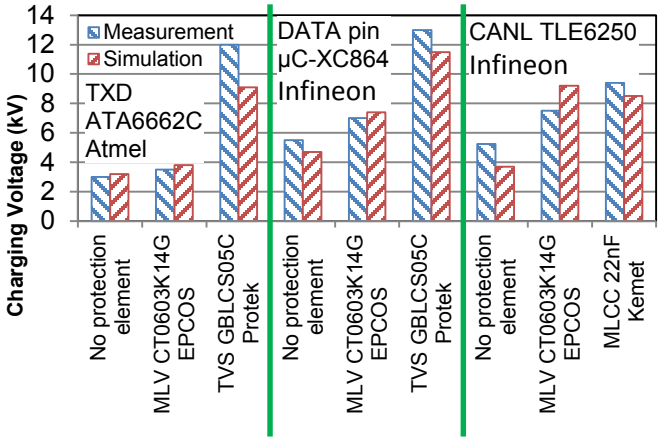

Fig. 17 Measured and simulated robustness on the system level levels in different configurations

C. SOA versus Thermal Failure Criterion

A narrow band filter as a protection circuit highlights the drawbacks of SOA criterion as proposed by SEED. A capacitor which is placed at the connector of the system in Fig. 18 is used in many designs. In combination with dynamic IC behavior and other PCB effects it may lead to oscillations. High voltage and high current peaks appear at an IC-pin in case of an ESD. The simulation results for the example configuration are shown in Fig. 19. The ESD robustness level using SOA in terms of current or voltage level as the failure criterion is unrealistically low because of oscillations and does not comply with measurement. Much more accurate results can be achieved by using the thermal failure criterion.

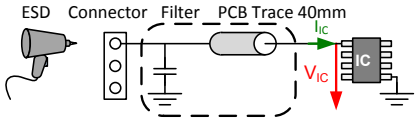

Fig. 18: Simulation setup for quantification of the impact of a narrow band LC-filter (15 pF and short PCB trace)

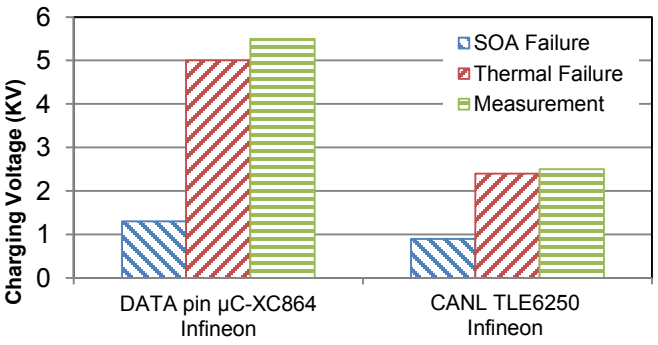

Fig. 19: Comparison of SOA and thermal failure criterion

IV. Simulation-Based Optimization of a Protection Strategy

In the previous sections simulation and measurement results were compared for example configurations and the applicability of the presented simulation approach could be verified. In the following section additional application examples showing the benefit of simulation in a system optimization process are presented.

A. Selection of Protection Element using the Frequency and I/V Curve

Often, a system's ESD requirement might only be met by using external ESD protection elements. For an appropriate selection operating frequency, operating voltage, size, and desired ESD robustness level, but also price must be taken into account. For finding the optimum protection strategy, the presented simulation approach can be very useful.

At first the IC has to be characterized as described in section II. The protection strategy might be roughly chosen considering the operating frequency. For low frequency applications an MLCC might be the best solution, but care has to be taken due to capacitance reduction at higher voltages. This behavior is considered using advanced MLCC models [26]. Nonlinear voltage-sensitive protection elements should be chosen if higher frequencies have to be transmitted. The most important criteria for the selection are the I/V curve and the capacitance. Ideally, there is no intersection in the I/V curve of the protection element and IC, whereas protection elements' breakdown voltage should be lower. The interaction of selected protection element, IC-pin, and the relevant ESD current path on PCB can now be simulated. The PCB trace between an IC and protection element can be especially important, to trigger the internal IC protection. Simulation will clearly state the ESD capability of the design and optimization measures can be found.

B. Protection of ICs with low Breakdown Voltage

Some ICs have very low breakdown voltage and the selection of a suitable protection element (as described) is more difficult because of functional issues. Decoupling of the protection element and the IC with a PCB trace can be a solution. For the avoidance of thermal failures, mainly the inductance has to be considered. Also in this case simulation can help to optimize a protection strategy (Fig. 20).

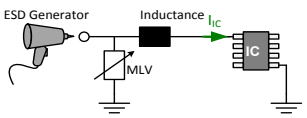

Fig. 20: Simulation setup for quantification of the impact of a PCB trace

The critical IEC system level stress is reached at 5 kV charge voltage for the modeled µC GPIO-pin. Simulation results are shown in Fig. 21 using the described configuration. The current amplitude and coupled energy were calculated under variation of the decoupling inductance in the range 1 nH to 100 nH. A MLV is used as the protection element. A PCB trace provides a high impedance discharge path for high frequency content of a signal. MLV is turned on due to the initial peak. The energy is reduced to 90% by an inductance of 10 nH, to 60% by using 100 nH in the discharge path.

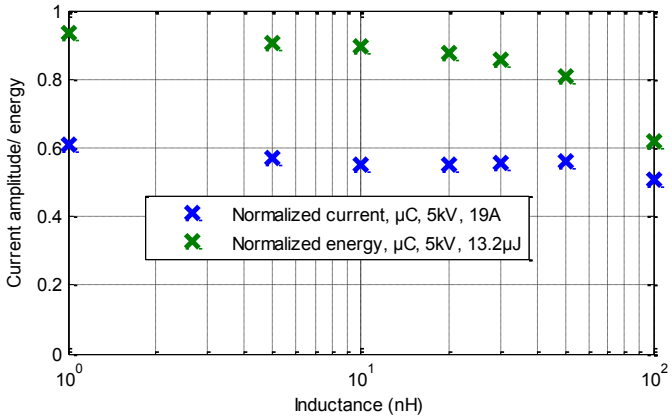

Fig. 21: Current amplitude and energy vs. inductance. Values are normalized to the initial maxima without ESD discharge

C. Selection of Grounding Configurations

Many applications have non-ideal grounding conditions, e.g. an automotive ECU that is connected to the car body by a longer cable.

A simplified setup demonstrates the effects to be expected. A middle-sized ECU is connected via a 1 m (considering thermal failures a simple inductance of 1000 nH is sufficient here for modeling) cable. The ECU enclosure and car body build a capacitance in the range of few pF. The exact value depends on physical dimensions of the setup. 5 pF is a typical value. In comparison to the discharge capacitor of the IEC generator the 5 pF of the ECU have low impact on thermal failure behavior. Four parameter sets regarding capacitive and inductive connections to the ground are shown in Fig. 22 and the impact on the ESD current injected to an IC-pin is analyzed.

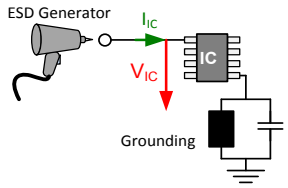

Fig. 22: Simulation setup for quantification of the impact of different grounding conditions

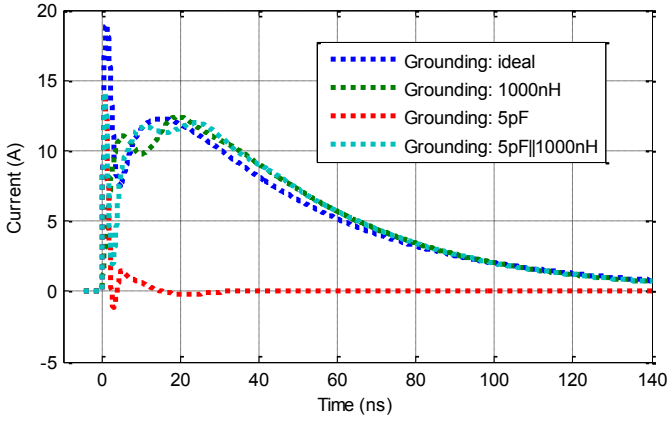

Fig. 23: Simulated current for 5 kV charging voltage on µC-GPIO with different grounding conditions

The floating ECU with only capacitive grounding is more robust against ESD stress in terms of thermal failure modes.

Anyway, the maximum voltage allowed for the IC is exceeded if the SOA criteria are used, but no thermal failure can be detected. The ground connection via a cable significantly attenuates the first current peak. Its effect on thermal failure is negligible. The system level robustness drops to approximately 5.1 kV. In case of capacitive and inductive grounding the current peak is slightly reduced, but the shape of the second peak of the discharge remains stable, which contains most of the energy stored in the capacitor of the ESD generator. In the simulation, IC failure is indicated at a testing level of approximately 5 kV charging voltage. IEC robustness for different groundings is shown in Fig. 24.

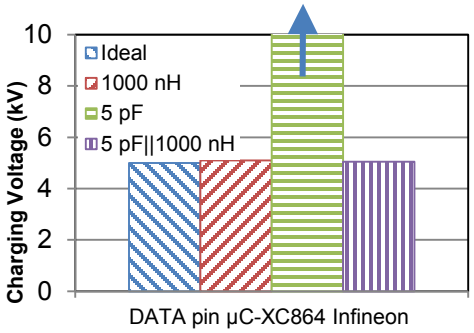

Fig. 24: Robustness on system level of µC-GPIO for different grounding

V. Conclusion and Discussion

A methodology for the simulation of thermal ESD failure on system level including ESD generator, protection elements, PCB traces, and the IC have been presented. A black box modeling approach (without any knowledge about IC or protection element design) has been successfully applied to multiple devices. Different failure mechanisms in ICs demand different failure models. In this paper it was found that thermal failure models can reproduce in many cases the ESD behavior of real systems. In contrast to overvoltage and overcurrent used in SOA pulse shape is integrated.

In some cases the described approach might face problems due to additional current paths enabled, when, e.g. the IC is used in a special configuration or internal ESD protection structures are not connected directly to supply or ground. Another limitation of the thermal model can be overvoltage failures. Here an additional overvoltage criterion has to be added. The proposed behavioral models also do not consider self-heating of the components during an ESD event which might change electrical and thermal properties significantly during an ESD. The limitations might cause the method to fail in some cases. However, in this paper many randomly selected IC configurations were analyzed. It could be shown that, at least for the automotive ICs, the simulation accuracy is high and sufficient for solving system design problems.

With the proposed method, a system designer is able to perform a trial and error optimization process virtually. A significant reduction of time to market can be achieved. The application of the presented thermal failure modeling method for other pulses e.g. Surge and Burst is very attractive. This will be subject of further research.

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