On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD

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Abstract - ESD protected LDMOS transistors show sensitivity to voltage overshoots. The pn-diode, nLDMOS and the combination are investigated in detail. The unique failure mode is identified as ongoing triggering of the parasitic bipolar transistor beyond a rise-time-dependent voltage overshoot of the ESD diode. Solutions for enhanced ESD protection are presented.

I. Introduction

Voltage overshoot due to turn-on behavior of ESD protection elements often shows a negative impact on ESD hardness and has become a matter of concern in design of advanced CMOS circuits for years [1, 2]. Harmful overshoots are reported in low voltage technologies, mainly causing damages at thin gate-oxide. In the field of high voltage (approx. 20V-100V) ESD protection, breakdown of thick gate-oxide is normally not a critical issue in ESD design. However, lateral DMOS (LDMOS) transistors as snapback ESD protection structures are believed to be inherently weak depending on device sizes [3, 4]. In fact, as the voltage reaches the region in excess of safe operating area (SOA), current filaments can occur at the onset of snapback accompanied with the danger of local burnout. Transmission line pulses (TLP) within only several nanoseconds pulse duration actually result in destructive LDMOS snapback in case the critical voltage and current are reached [5]. Voltage overshoots can induce locally thermal overload in DMOS devices and thus have to be considered.

To avoid the triggering of the parasitic bipolar transistor in LDMOS, voltage clamping devices such as avalanche pn-diodes are usually applied and connected in parallel to protect the weak LDMOS transistors with the upper limit of the ESD window given by the trigger voltage (V_{t1}). Avalanche pn-diodes as protection devices belong to static-triggered voltage clamps. Thus, the robustness of a standalone pn-diode has no dependence on rise-time of the ESD pulse. However, TLP tests showed this type of on-chip protection concepts do not provide the expected ESD hardness especially during the TLP tests with short rise-times.

To address this problem, this work presents the case studies of four different high voltage ESD test structures and explores two different failure modes in these concrete examples. Many measurement and simulation results are carried out accompanied with the detailed investigation of the n-type LDMOS as the device being protected. Device simulation was utilized to identify the unique failure mode of the LDMOS transistor as ongoing bipolar triggering. Suggestions of more efficient ESD protection for voltage sensitive circuits against stresses with fast transients are provided as well.

II. Case Studies and TLP Results

Fig. 1 shows the schematic diagrams of the studied test structures, which are very representative in the field of high voltage ESD applications. The nLDMOS transistor with two different gate biasing conditions is protected with an avalanche ESD diode connected in

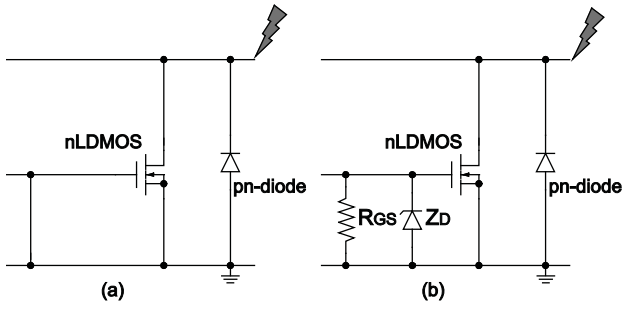

Figure 1: Schematic diagram of the tested structures: (a) gg-nLDMOS, (b) gc-nLDMOS with Zener protection on gate.

parallel. In the grounded-gate (gg) configuration, gate and source are tied to ground. In the gate-coupled (gc) configuration, R_{GS} is designed to achieve a discharge time constant $R_{GS}C_{GS}$ of about 100ns, which allows the transient gate-biasing of the transistor on a certain level during the stresses (e.g. pulse width t_w=100ns). A Zener diode (clamping at 10V) is used as overvoltage protection of the gate-oxide. In both cases, gate-oxide will not be initially damaged during ESD events. Note that all the interconnections are kept very short with negligible parasitic effects.

For each circuit configuration two nLDMOS with different channel width (ratio 68:1) were implemented. The smaller nLDMOS can only divert current in the milliamp range with insignificant contribution in ESD performance, while the larger nLDMOS has a certain capability of self-protection. The ESD diode, characterized with standard TLP, is used to clamp the voltage across the nLDMOS and to keep it below the voltage limit determined by the electrical SOA of the transistor with the specified ESD ruggedness (current level corresponding to 4kV HBM in this case study).

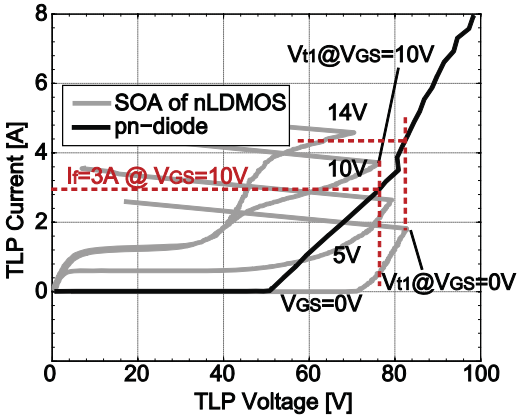

Figure 2: SOA of the large nLDMOS with gate-biasing from 0V to 14V and I-V characteristics of the pn ESD diode. Dashed lines show the current levels merely due to ESD diode at different SOA limits (V_{t1}). Devices are tested using standard TLP with t_r=10ns, t_w=100ns. The averaging window is 70ns to 90ns.

Fig. 2 illustrates the pulsed SOA of the large nLDMOS used in the test structures overlapped with the I-V characteristic of the ESD diode. Note that even by neglecting the current diverted through the larger transistor, the pn-diode should provide sufficient ESD robustness. In the case of gc-nLDMOS for example, V_{t1} is smaller with V_{GS} of 10V compared to the case of zero V_{GS}. As the current through the ESD diode is approximately 3A at the voltage drop equal to V_{t1} with V_{GS}=10V, the failure current of the test structure can be estimated at least at 3A as well. By assuming the correlation between 100ns TLP and HBM, in the worst case scenario of small nLDMOS in the gc-configuration, the current level is expected to be larger than 4kV HBM (2.67A). Since the pn-diode works as a static-triggered ESD protection element, no dependence on rise-times was expected in the test structures.

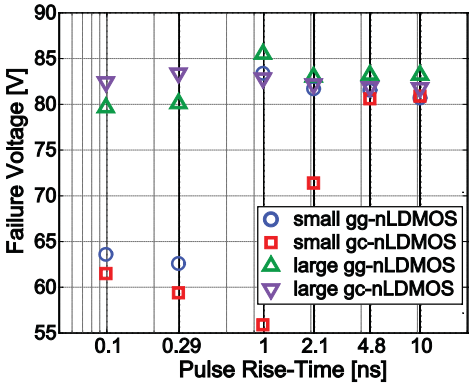

Figure 3: Failure voltage of the four test structures (Fig. 1) versus TLP pulse rise-time.

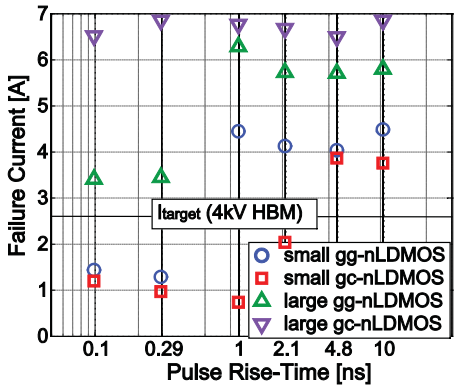

Figure 4: Failure current of the four test structures (Fig. 1) versus TLP pulse rise-time.

As a matter of fact, the target ESD performances are not achieved during the experiments. Fig. 3 and Fig. 4 show the strong dependence of failure voltage and current on rise-times (t_r). TLP measurements are performed using different t_r but the same t_w=100ns with the averaging window from 70ns to 90ns. For t_r larger than 4.8ns, failure voltage and current meet the values which can be easily predicted by using the TLP characterizations of the stand-alone pn-diode and nLDMOS. Under shorter rise-times however, failure levels of the structures with smaller nLDMOS are far below expectation and with large fluctuations. For the large gg-nLDMOS, the ESD performance is lower when rise-times are in sub-nanosecond range. Note that the early failures of these test structures are measured in TLP tests without any pre-pulse voltage (PPV) on the discharge pins. The harmful avalanche breakdown delay of the pn-diode or DMOS described in [6] due to PPV is not the cause of the unexpected results.

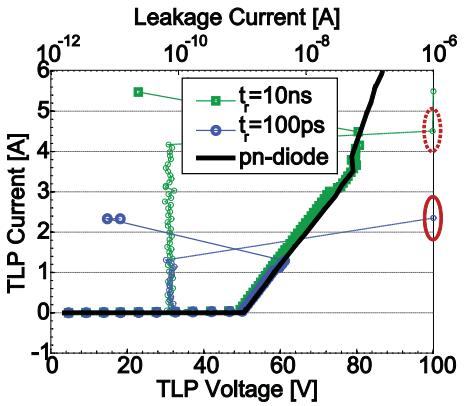

Figure 5: TLP characteristics with the leakage current plots of the small gg-nLDMOS tested with t_r=10ns and 100ps. The averaging window is 70ns to 90ns with t_w=100ns. I-V curve of the pn-diode is also shown. Different failure levels are indicated.

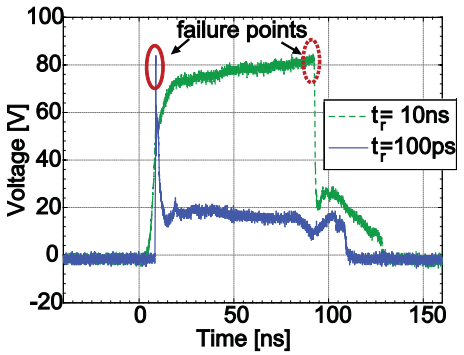

Figure 6: Voltage waveforms of the pulses causing failures of the small gg-nLDMOS structure with t_r=10ns and 100ps. Failure points are at completely different time instants.

In addition to the failure voltage and current derived from averaged TLP pulses, the transient waveforms are of great interest. As an Example, the TLP results of the small gg-nLDMOS with expected and so-called early failures are illustrated in more detail in Fig. 5 and Fig. 6, representing the two different failure modes. As the nLDMOS barely conducts transient current, TLP characteristic of the small gg-nLDMOS must correspond with the pn-diode until the LDMOS fails. For t_r=10ns, the failure occurs at the end of the pulse due to exceedance of the electrical SOA. The nLDMOS is driven into the destructive snapback condition. For t_r=100ps on the other hand, early failures are always found at the very beginning of TLP stresses. They can be related to the voltage overshoots. The failure levels of early failed devices are significantly lower.

III. Study on the Dynamic Issues

A. Test Artifacts in TLP

Before addressing the causes resulting in the early failures of the test structures, test artifacts must be evaluated. The 4-point probes method [7] was applied in the TLP measurements as shown in Fig. 7. The sense needle with integrated 1kΩ resistor provides a measurement bandwidth of about 7GHz taking account of parasitic capacitances. The parasitic effects caused by the inductances, primarily the mutual inductances (L_P), are quantified with an on-chip short. The voltage spikes induced merely by the inductive couplings are very scalable and rather small as depicted in Fig. 8. For instance, the on-chip short with 4A TLP current only produces a voltage overshoot of 1.2V. Voltage overshoots with large amplitude are thus not due to test artifacts.

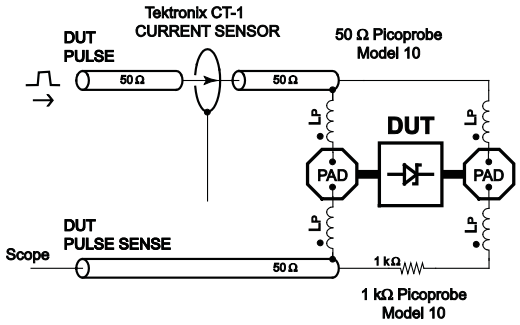

Figure 7: Wafer measurement configuration using 4-point probes method.

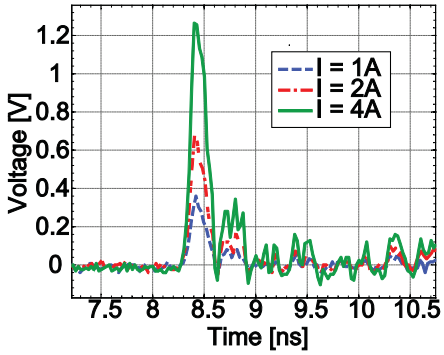

Figure 8: Inductive coupling tested for different current levels with an on-chip short.

B. Overshoots of Avalanche pn-Diodes

From the TLP results, the nLDMOS as the device being protected suffers from early damage despite the ESD diode. Therefore, the detailed analysis of the protection diode must focus on the avalanche breakdown process. The mean avalanche propagation speed when the current reaches its final value is rather fast and given by [8]. Depending on device geometry, the propagation time is very short (picoseconds to tens of picoseconds), representing the duration from high to low ohmic state of the diodes. However, the time until a free charge carrier becomes available to initialize the avalanche multiplication is statistically distributed. The result is voltage overshoot which exceeds the static breakdown voltage. Fig. 9 shows the voltage spikes of the stand-alone pn-diode under

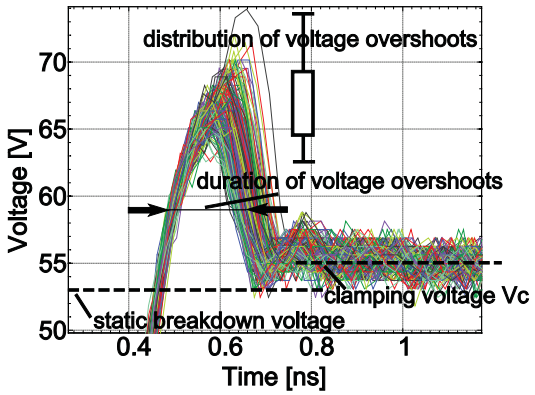

Figure 9: Voltage overshoots observed by testing the stand-alone ESD pn-diode with TLP (t_r = 100ps). Same test is repeated 200 times in order to illuminate the distribution.

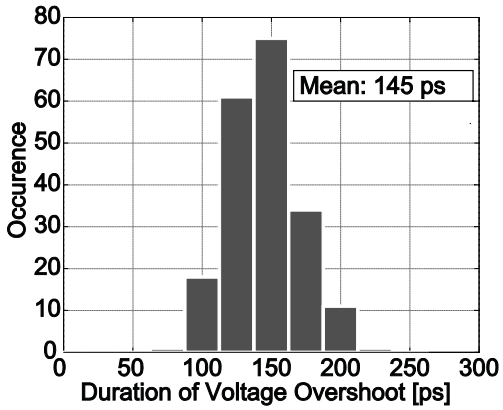

Figure 10: Statistical distribution of the overshoot duration according to Fig. 9. Mean overshoot duration is about 145ps.

TLP tests with t_r=100ps and a TLP current of 1A. The voltage waveforms are recorded using an oscilloscope with 40GS/s sampling rate. The scattering in the rising edge of the pulses is much smaller than in the falling edge of the overshoots. Hence the different duration of voltage overshoots does not originate from fluctuation of the oscilloscope but is mainly due to the pn-diode itself. Fig. 10 gives the statistical distribution of the overshoot durations. A faster triggering to avalanche breakdown produces a lower voltage peak. Note that the voltage peaks (over 10V at 1A TLP current) vary in a relatively wide range and cannot be test artifacts as discussed earlier (Fig. 8). It is also observed in the measurements that the average overshoot duration decreases with increasing TLP current because the peak voltage (V_p) is larger with a higher chance to find a free carrier to launch the avalanche multiplication (Fig. 11). And vice versa, the time until a free charge carrier becomes available gets shorter, resulting in the smaller increase of V_p at higher current levels ($\Delta V_{p2}<\Delta V_{p1}$). On the other hand, the average V_p is getting smaller with the longer rise-times at the same TLP current level. With rise-time above 5ns, no significant overshoot can be detected

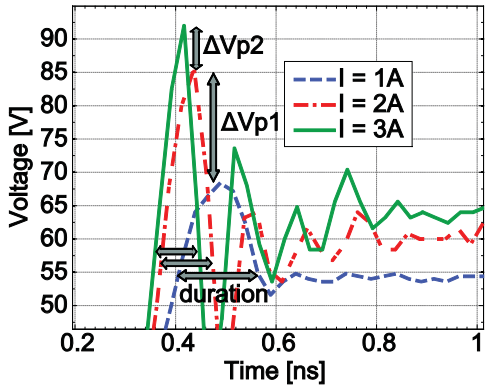

Figure 11: Voltage overshoot and its duration as a function of TLP current levels with the same rise-time of 100ps.

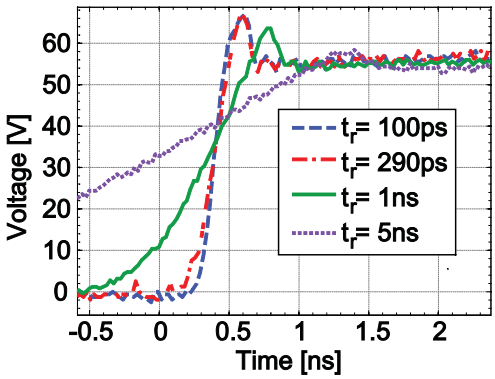

Figure 12: Voltage overshoot as a function of rise-times with 1A TLP current. t_r=100ps and 290ps show almost the same slope because of the parasitic capacitance of the pn-diode.

(Fig. 12). As a result, voltage overshoot on avalanche pn-diode is an inherent behavior, which should be carefully characterized and controlled in high voltage ESD designs, even without the existence of pre-pulse voltage.

C. Transient SOA of nLDMOS

Since it is believed that the voltage overshoot studied in the stand-alone pn-diode plays an important role in the early damages in the test structures, the SOA of the nLDMOS with different device sizes is further investigated especially in short-pulse range. The term transient SOA introduced in [9] is also tested in this work using vf-TLP setup with TDR method [10]. The measurement results are shown in Fig. 13. V_{GS} is biased on 0V and 10V, corresponding to gg- and gc-configuration in the test structures, respectively. It is found that rise-times do not have considerable impact on V_{t1}. The triggering of the inherent bipolar transistor in the nLDMOS as a function of dV/dt is not observed.

In other words, the SOA of nLDMOS itself is not affected by rise-times but is limited through absolute values of drain-source voltage. Note that V_{t1} of the large nLDMOS should be smaller than the measured

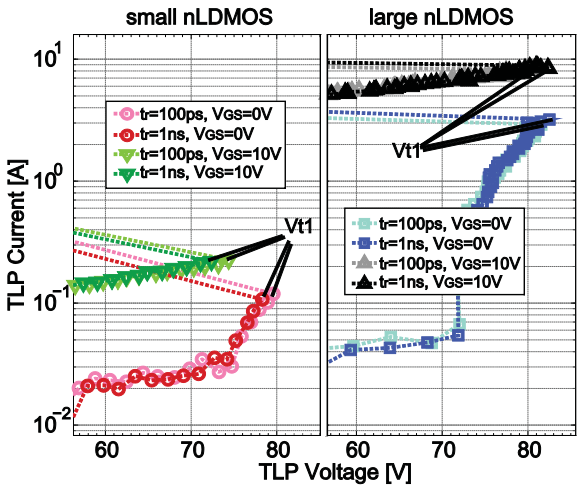

Figure 13: Transient SOA tested with 5ns pulse width vf-TLP for a (left) small and a (right) large nLDMOS transistor.

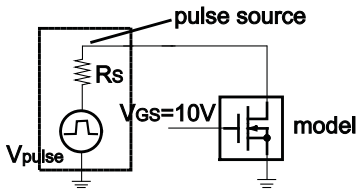

Figure 14: Schematic of simulation setup. In voltage conditioned simulation, V_{pulse} and R_s are set smaller representing the SOA measurement for the small nLDMOS. In current conditioned simulation, V_{pulse} and R_s are set larger representing the measurement for the large nLDMOS.

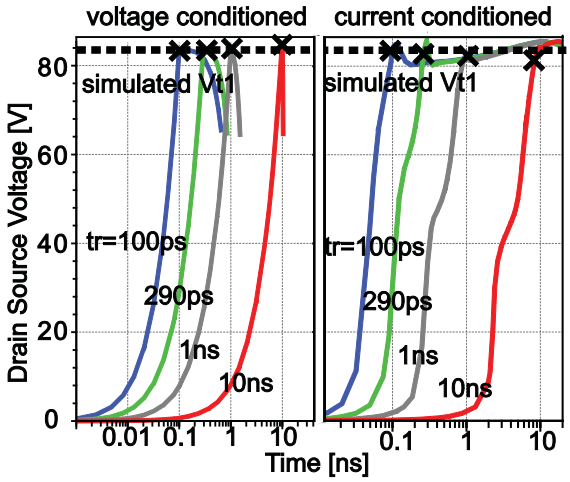

Figure 15: Simulated voltage waveforms of (left) voltage and (right) current conditioned setups with V_{GS}=10V and various pulse rise-times. V_{t1} is marked by "X", showing a fairly constant trigger voltage.

values since the contact resistance between the pulse needle and device pad is not de-embedded from TDR setup.

In addition to the SOA characterizations using vf-TLP, the time evolution of the bipolar triggering inside the transistor is investigated by device simulation. The commercial SDEVICE simulator by SYNOPSYS [11] is used. The simulation setup is schematically shown in Fig. 14 with V_{GS}=10V. For the test structures with smaller transistor, the charged TLP cable acts like a voltage source since the nLDMOS exhibits much larger impedance compared to the 50Ω system. For the structures with larger transistor, TLP becomes more like a current source since the impedance of the test structures is smaller than the impedance of the TLP system. Both cases are reproduced in the transient simulation.

The pulse source acts as a voltage or a current source like in the TLP measurements by setting the resistance R_s according to

$$R_s = 50\Omega \cdot DUT\ width/model\ width\,. \quad (1)$$

Fig. 15 displays the simulated voltage waveforms. Note that in voltage conditioned simulation, the pulse source as a voltage source is only valid before the bipolar triggering due to a substantial increase of current. On the other hand, the V_{DS} snapback is not visible immediately after the bipolar triggering in current conditioned simulation due to current limitation. Furthermore the nLDMOS is an ideal homogenous device in this 2-D device simulation not allowing current filamentation. The triggering of the bipolar transistor can however be determined by inspecting the device cross section [5]. The time instants when the triggering occurs are indicated with "X" in Fig. 15. According to the results, the bipolar triggering of the nLDMOS is purely electrical in sub-nanoseconds to nanoseconds range. Trigger voltage and current under voltage- and current-biasing conditions do not change with rise-time. Note that simulation is not calibrated with experimental data, hence without good agreement of V_{t1} values. Based on experiments and simulations, the nLDMOS is not directly affected by shorter rise-time (dV/dt or dI/dt) effects. The reduction of the ESD performance of the tested structures must be caused by rise-time dependent voltage overshoots of the pn-diode.

The qualitative agreement between experiments and simulations here verifies additionally the used simulation setup as reliable.

D. Ongoing Triggering of Parasitic Bipolar Transistor in nLDMOS

Fig. 16 shows the transient response of the pn-diode and a small nLDMOS to a 5ns long TLP pulse. The well-designed ESD diode exhibits overshoots only for several hundreds of picoseconds and rapidly clamps the voltage to a lower value than V_{t1}. In this particular example, the nLDMOS snaps back and sustains the 5ns current without being damaged due to

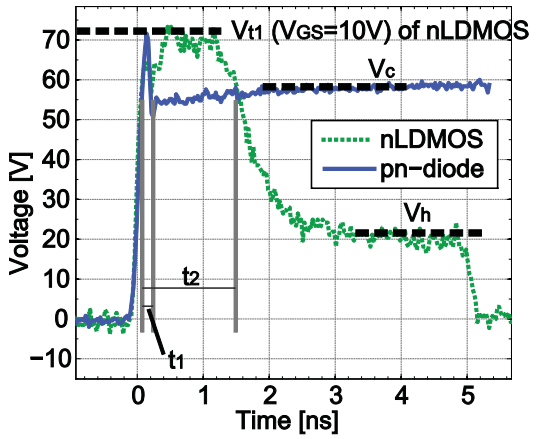

Figure 16: Transient response of a stand-alone pn-diode showing an overshoot reaching V_{t1}. Voltage waveform of a stand-alone small nLDMOS in snapback is also shown. The nLDMOS is stressed by 5ns long TLP without destruction. Gate-source voltage is biased on 10V. Both devices are independently measured and the waveforms are time-aligned for comparison.

homogenous current flow. It is clearly shown that the clamping process of the ESD diode is much faster than that of the LDMOS snapback (t1<t2). It could be expected that the process of snapback in the nLDMOS transistor is stopped before local burnout occurs if the voltage drop across the pn-diode falls from its peak value quickly below V_{t1}. This is obviously not always the case according to the early failures in our case studies discussed before.

To understand why the transistor suffers early failure due to voltage overshoots, the study on the interaction of the pn-diode and nLDMOS is necessary. Transient thermo-electrical TCAD device simulation is

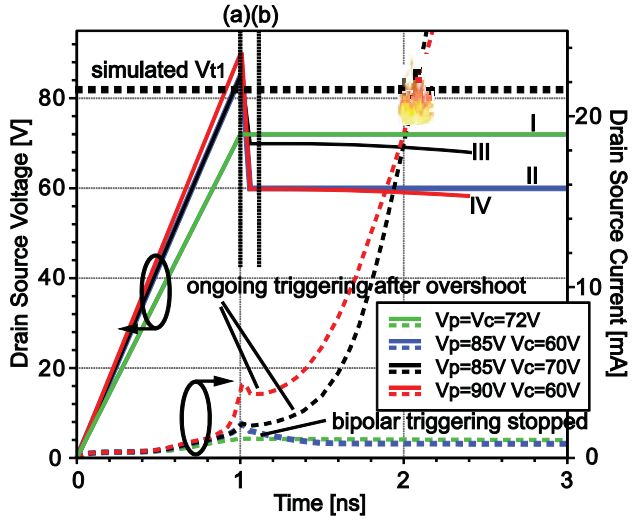

Figure 17: Voltage overshoots applied to the nLDMOS with V_{GS}=10V in simulation. The unique failure mode where the bipolar triggering cannot be turned off depends on V_p, V_c and is identified by the current waveforms. Local burnout due to the temperature rise is indicated. This behavior leads to the term dynamic destruction of the nLDMOS beyond voltage overshoots.

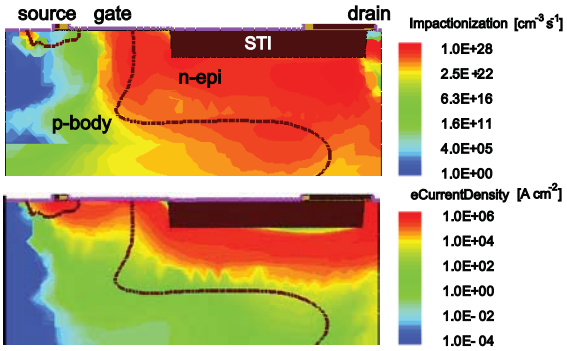

Figure 18: Simulation results of (top) impact ionization and (bottom) electron current density at time instant (a) in Fig. 17 for V_p=85V.

performed to give insight into the detailed physical behavior of the transistor in the first few nanoseconds. Fig. 17 shows current responses of the nLDMOS biased at V_{GS}=10V to voltage stresses with different peak voltage (V_p) and clamping voltage (V_c). The voltage pulses are applied to the transistor with 1ns rise-time and with only 10ps peak duration. The fall-time from V_p to V_c is set to 50ps corresponding to the previously found avalanche propagation time. This voltage conditioned simulation is oriented to the small gc-nLDMOS test structure.

If the maximal voltage remains at 72V (case I) which is below V_{t1}, the bipolar triggering does not happen as expected. In case II (V_p=85V and V_c=60V), the parasitic bipolar transistor is initially activated and then turned off due to the lower clamping voltage. However in case III (V_p=85V and V_c=70V), the triggering starts in the same way as in case II but is not stopped due to the higher V_c. The result is device destruction even though V_c is much lower than V_{t1}. This transient simulation actually reflects the voltage overshoots due to the pn-diode and the destructive

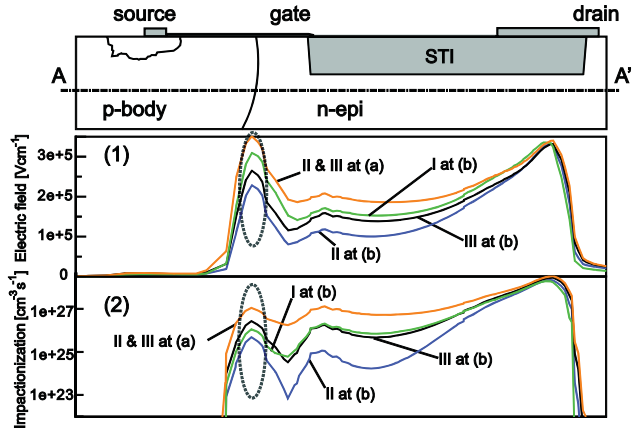

Figure 19: (Top) Cross section of the nLDMOS. (Bottom) Along the cutline A-A', (1) electric field and (2) impact ionization at V_{GS}=10V for cases II & III at time instant (a), case I at time instant (b), case II at time instant (b), and case III at time instant (b), respectively.

bipolar triggering.

Fig. 18 shows impact ionization and electron current density for cases II and III at the same time instant (a) in the device cross section. Strong impact ionization results in large generation of electron-hole pairs in the region around the STI. Large amount of electrons injected from source to body clearly indicates an active bipolar triggering in the nLDMOS transistor.

Fig. 19 depicts a comparison of electric field and impact ionization for cases I, II and III at the different time instants (a) and (b) along the cutline beneath the STI. At time instant (b), the voltage is clamped to V_c and the electric field is higher in a larger area for case III compared to case II. The higher electric field in case III provides larger impact ionization and hence more holes in the p-body. The hole current further biases positively the base-emitter junction, resulting in more electron injection from the source. This keeps the bipolar triggering process ongoing due to a positive feedback. It leads to a drastic increase of current until thermal destruction. On the contrary, when the clamping voltage is below the critical level, impact ionization is not able to keep the bipolar triggering process ongoing. The current level then returns to the status where $V_{DS}=V_c$ as shown in case II.

Compared to case III, the electrical field for case I at the indicated location in Fig. 19 is stronger due to higher electrical potential. The impact ionization is however lower in the important p-body/n-epi junction region without reaching the critical level. This is because impact ionization rate is not only a function of electric field, but also depends on current density [12]

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q}. \qquad (2)$$

α_n and α_p denote ionization coefficients of electrons and holes which are strongly dependent on electric field. J_n and J_p are electron and hole current densities, respectively. In case III at (b), the ionization rate is above the critical level due to the existing current flow generated by the previous voltage overshoot. Hence impact ionization is the key parameter which determines whether the process of ongoing triggering takes place.

In addition to the clamping voltage V_c, the unique process also depends on the precondition V_p. In the case IV with the same V_c=60V as in case II but a larger V_p=90V, the bipolar triggering does not terminate and dynamic destruction of the nLDMOS occurs due to the higher current density and impact ionization at time instance (b) caused by the previous larger voltage overshoot (Fig. 17).

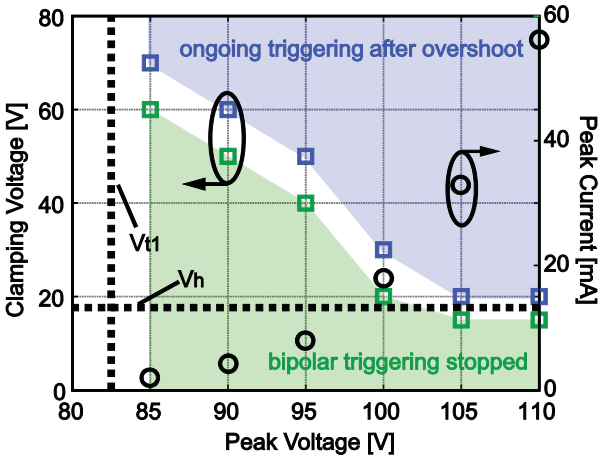

Figure 20: The critical condition for the nLDMOS for ongoing bipolar triggering based on the same transient simulation as described in Fig. 17 with different combinations of V_c and V_p. The rise-time of the voltage pulses is 1ns and the peak duration 10ps. The transistor is biased with V_{GS}=10V. Peak current as a function of V_p is also shown.

In an overview, the critical condition for ongoing triggering after a voltage overshoot as a function of V_c and V_p is shown in Fig. 20 based on device simulation. At higher V_p, V_c must be lower to avoid ongoing triggering. As an example, if a pn-diode as ESD protection provides a fast clamping at 50V, a voltage overshoot above 95V is not allowed. If V_c is below V_h, ongoing bipolar triggering does not occur in the investigated range of V_p.

The peak current I_p is defined as the drain-source current when the voltage reaches V_p. The higher the peak voltage, the larger the peak current is expected due to larger impact ionization at time instant (a). Hence from equation (2), the situation becomes more critical, requiring a lower V_c to start a recovery process from bipolar triggering. Again, the level of impact ionization determines if bipolar triggering is ongoing or a recovery process takes place in the nLDMOS transistor.

Of course for voltage stresses with other rise-times instead of 1ns, ongoing triggering as a function of V_c and V_p is different in general due to different I_p.

The effect of ongoing bipolar triggering is also observed in the gg-configurations (V_{GS}=0V) in simulation. The formation of ongoing triggering process depending on V_c and V_p is not as critical as in gc-case since the overall current density is lower without MOSFET channel current. Together with larger V_{t1} (Fig. 13), it is clear that the smaller gg-nLDMOS becomes less sensitive to overshoots as shown in the TLP results (Fig. 3 and Fig. 4).

Fig. 21 summarizes measured transient waveforms of the stress to failure in the first nanoseconds for small

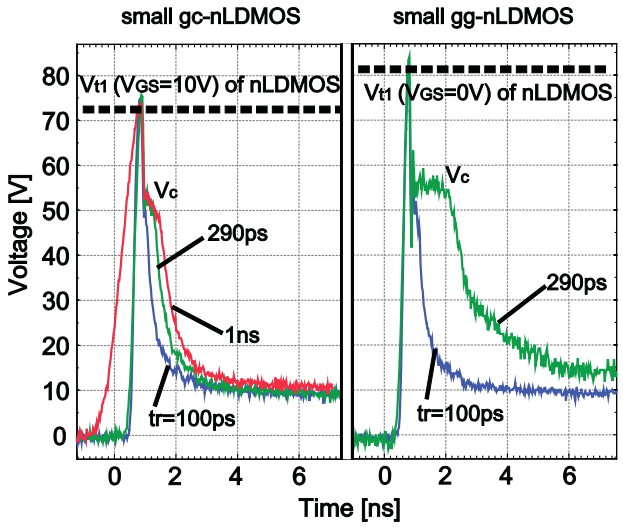

Figure 21: Waveforms of stresses to failure regarding voltage overshoots for small (left) gc- and (right) gg-nLDMOS configurations with various rise-times. Ongoing triggering is launched, causing dynamic destruction. The curves are time-aligned according to the voltage peak for better comparison.

gg- and gc-configurations. The waveforms demonstrate the dynamics of ongoing triggering. After the overshoot, the voltage is initially clamped to V_c for a short time. Then a further voltage reduction to approximately 10V becomes visible. This is the destruction of the nLDMOS because the voltage falls lower than the non-destructive holding voltage shown in Fig. 16. The duration of destruction can be related to the rise-time at least for the same test structure. The longer the rise-time, the longer takes the destruction process. A possible reason is the effect of rise-time on initial distribution of current filaments [13]. The shorter rise-time induced current filaments can be multiple and delocalized in the small nLDMOS, resulting in stronger heating and faster thermal damage under the stress of a voltage conditioned pulse source.

IV. Failure Analysis, HBM Results and Improvement Proposals

In the previous sections of this paper, two failure modes have been investigated. Even if the electrical mechanisms have been shown to be of quite different nature, they both lead to a snapback of the parasitic bipolar transistor. The remaining pulse delivers enough energy to cause thermal destruction of the silicon due to current filament and Joule heating in the end. To confirm this, two samples have been analyzed by failure analysis, one sample with an expected and the other with an early damage in the small gc-nLDMOS. Fig. 22 shows the results: the damages of

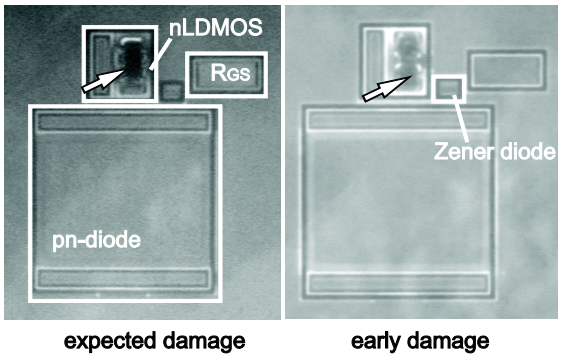

Figure 22: Failure analysis of (left) expected and (right) early damage in the test structure small gc-nLDMOS caused by 100ns TLP tests. Both pictures show the final result of thermal run-away in the nLDMOS.

both failure modes are located in the nLDMOS without any substantial difference.

In addition to the TLP characterization, standardized HBM tests have been performed. Thereto, the studied circuits are encapsulated in the LQFP plastic package with 64 pins. The measurements are performed on a KeyTek ZapMaster HBM tester. In order to avoid PPV effects reported in [6, 14, 15], a 10kΩ shunt resistor is connected to discharge and ground pin.

Table 1 shows the test results for the four test structures. The circuits do not have a crucial problem with voltage overshoots and all structures pass at least 3.5kV HBM stress. It is believed that parasitic capacitance in the HBM tester, test board, socket and package modulates the voltage rise-time to safe levels. However, in the case of real human body discharges with lower capacitance in discharge path, reduction of the ESD performance due to overshoots can happen. The initial front rise (IFR) of the HBM pulse can be much shorter than 10ns since it is given by the time needed for the voltage rising from zero volts to the breakdown voltage of protection element [16, 17]. Hence voltage overshoots induced early damage remains a potential danger in this ESD protection concept in the test structures. Further, for ESD requirements such as CDM, CDE and IEC 61000-4-2 with shorter rise-times in high voltage applications, overshoot sensitivity of the ESD protection as shown in this case study can lead to unpredictable performance thus must be prevented.

Table 1: HBM results of the test structures in LQFP-64 package.

	highest pass level	lowest fail level
small gc-nLDMOS	>6kV	5.5kV
small gg-nLDMOS	>6kV	4kV
large gc-nLDMOS	>6kV	6kV
large gg-nLDMOS	>6kV	4.5kV

The prevention of the voltage overshoot by increasing the capacitance between the discharge pins is the most straightforward solution. Wafer-level TLP measurements with additional capacitances (56pF for the weakest small gc-nLDMOS) connected in parallel to the test structures showed the successful suppression of the overshoots and hence the prevention of the early damages. This solution equals a transformation of the ESD pulse with an RC-filter into a pulse with longer rise-time. However, adding on-chip capacitances as an ESD protection method is area expensive and an off-chip capacitance is not always desired.

Another improvement possibility is the use of larger pn-diodes which have higher ESD capabilities in the same voltage class. They keep the voltage drop during the ESD stress at lower levels. A drawback is again the reduced area efficiency.

Advanced ESD protection concepts using active clamps [5, 18] instead of pn-diodes are a third solution. Due to the much faster turn-on of the channel current in large DMOS transistors, harmful voltage overshoots can hardly exist even with extremely short pulse rise-times (<150ps). Active clamps are area efficient and the PPV problem can be also handled. In our case studies, the large gc-nLDMOS showing overall good results actually confirms this type of solution (Fig. 3 and Fig. 4).

V. Conclusions

Voltage overshoots due to fast transients can lead to ongoing bipolar triggering in high voltage LDMOS transistors. This even happens due the overvoltage caused by the finite reaction time of the avalanche breakdown diode which is much shorter than the time for bipolar triggering in the nLDMOS transistor. The triggering of the nLDMOS transistor in the snapback mode results in significant degradation of the ESD protection's effectiveness. Rise-time (dV/dt or dI/dt) does not affect the bipolar triggering in the nLDMOS transistor directly but can certainly impact voltage overshoots. Development of overshoot-free ESD protection devices insensitive to rise-time effects is gaining more interest in order to eliminate early damages.

Acknowledgements

The authors would like to thank Reinhold Gärtner for enabling HBM tests and Thomas Schweinboeck for the failure analysis. The authors acknowledge fruitful discussions with the colleagues Filippo Magrini, Michael Mayerhofer and Alevtina Podgaynaya. Our grateful thanks also go to Chai Gill for her review and excellent mentoring work.

This work was supported by the MEDEA+ project 2T205 SPOT-2.

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